Impact of SiO_2 Cladding Voids in SiPh Building Blocks

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***Abstract*— The impact of buried air gaps (voids) in SiO_2 cladding in common silicon photonics building blocks is investigated through simulation. The void cross-sectional areas in devices fabricated through a commercial electron beam lithography process are evaluated and found to be less than 500 nm^2.**

Keywords—Air gaps, Silicon photonics, Directional couplers, Sub-wavelength grating (SWG).

I. INTRODUCTION

Silicon-on-Insulator (SOI) substrates are used to fabricate silicon (Si) waveguides, which guide light. A layer of SiO_2 covers the Si waveguide as the cladding, protecting the silicon layer and engineering the refractive index difference. In several components such as sub-wavelength grating (SWG) structures, fiber grating couplers, directional couplers, mode multiplexers, and ring resonator couplers, silicon structures in close proximity allow light to couple and permit engineering of the effective refractive index. In such cases, the SiO_2 upper cladding may not properly fill the gap between the silicon features, resulting in an air gap buried under the cladding. These air gaps, which we call voids, might change the experimental performance significantly depending on their volume, position, and shape. Their volume depends on the Plasma-Enhanced Chemical Vapor Deposition (PECVD) process of the cladding and the distance between the silicon structures. The characteristics of the fabricated design can considerably be different from the design values if those voids are neglected in the design phase. Voids can be considered in the simulation and design phase [1]. Here, we investigate through simulations the impact of voids on some common structures including fiber grating couplers, directional couplers, and SWG multimode interference (MMI) couplers. Experimental characterization of a broadband SWG MMI sensitive to voids fabricated through the Applied Nanotools (ANT) foundry is also presented.

Figure 1 shows an SWG structure, directional coupler, and ring resonator where there is a narrow gap between the silicon segments that the SiO_2 cladding may not be able to fill. The amount of trapped air is usually represented by the area of the void in longitudinal cross-section area of the device $(x \times y)$ as indicated in the inset of Fig. 1-a with the light guided in the x-direction.

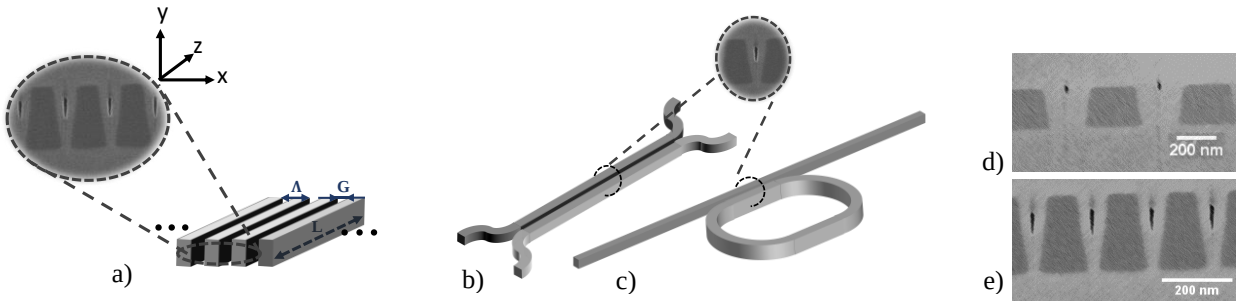

Fig. 1. a) A sub-wavelength grating structure where L is the length, G is the gap between the blocks, and Λ is the period of the grating; b) directional coupler; c) ring resonator. Insets: voids in the SiO_2 cladding measured via helium ion microscope (HIM) images of the voids in SiO_2 cladding prepared by a Ga-FIB from ANT. HIM images from ANT showing: d) small voids; e) worst-case voids with area less than 500 nm^2.

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II. Impact of Voids on SiPh Building Blocks

There are several SiPh building blocks susceptible to the impact of voids. Sub-wavelength grating couplers are among one of the most well-known solutions to implement fiber to chip coupling. Equation 1 presents the central wavelength (λ) as a function of the effective index of the SWG structure (n_{eff}), the refractive index of cladding (n_c), and the light output angle from cladding (θ_c) [2].

$$\lambda = \Lambda(n_{eff} - n_c \sin\theta_c) \quad (1)$$

The presence of voids lowers n_{eff} and, consequently, the central wavelength for a fixed output angle of light. Figure 2-a shows the shift of the peak wavelength relative to different volumes of voids. The directional coupler presented in Fig. 1-b usually has trenches with a width ranging from 100 to 150 nm. Results in Fig. 2-b show the impact of voids on peak wavelength transmission. The SWG MMI shown in Fig. 2-c is a solution to get ultra-broadband flat response over a 300 nm wavelength. However, the presence of voids causes additional loss, especially in the cross port of the MMI coupler. The structures are simulated with voids' area ranging from 3500 nm^2 to 7500 nm^2 which are realistic numbers in processes and reported in [1].

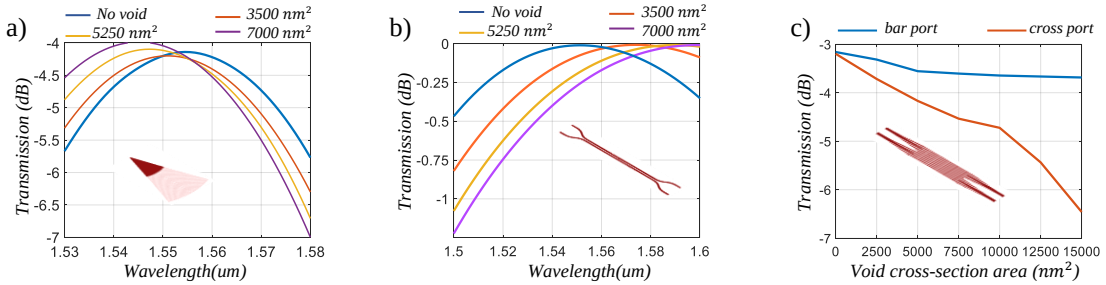

Fig. 2. Simulation results of the impact of voids for different SiPh building blocks: a) grating coupler; b) directional coupler; c) simulation of transmission response of a SWG MMI design with respect to different voids cross-section area at $\lambda = 1550\ nm$.

III. Experimental Results

To assess the presence of voids in the ANT electron beam lithography (Ebeam) fabrication process, characterization of a broadband SWG 2×2 MMI power splitter is presented. The design in Fig. 3-a is derived from [1]. The simulation results presented in Fig. 3-c show the excess loss of the structure with respect to different void cross-sectional areas in the cladding of the structure. The voids are modeled in simulation as shown in Fig. 3-b. Characterization results of the fabricated structure (solid blue line in Fig. 3-a) align with simulation results considering no voids in the cladding. We conclude that there is not a considerable volume of voids in the cladding. The later FIB-HIM study on sub-wavelength structures with various gaps (G in figure 1-a) fabricated through this process confirmed this finding. It is worth noting that a thin coating of at least 10 nm of silicon dioxide on all silicon features may be preventing the voids from directly contacting the silicon features which likely reduces the impact of the voids.

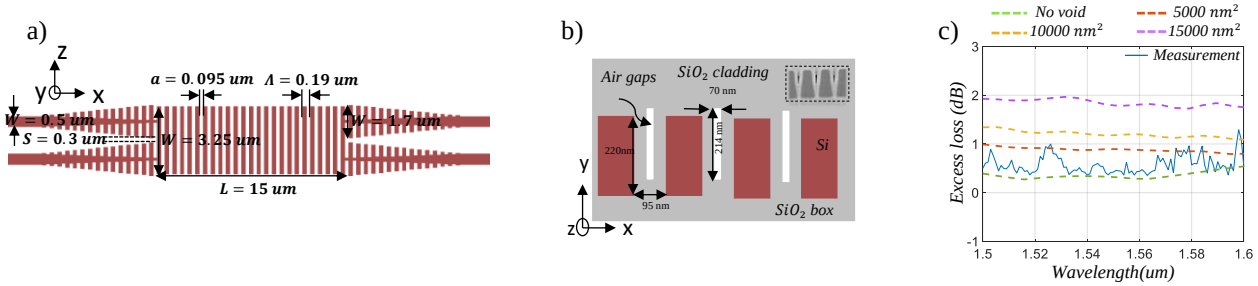

Fig. 3. a) The layout of the simulated and fabricated SWG MMI; b) side-view of the structure showing modeled 15000 nm^2 upper cladding voids; c) measured and simulated performance of the broadband MMI where the blue line shows the experimental characterization of the structure fabricated through ANT and each dash line represents the simulated excess-loss of the MMI considering different void cross-sectional areas in the upper cladding of the chip.

IV. Conclusion

The above-mentioned voids, depending on their volumes, may have a critical impact on silicon photonic (SiPh) designs where close proximity silicon blocks exist. Their volume depends on several factors including the distance between silicon blocks and the PECVD deposition of the fabrication process causing significant fabrication non-uniformity effects between processes. When void cross-sectional area exceeds 1500 nm^2, they must be taken into account at the design phase.

[1] Halir, Robert, et al. "Ultra‐broadband nanophotonic beamsplitter using an anisotropic sub‐wavelength metamaterial." Laser & Photonics Reviews 10.6 2016, 1039-1046.

[2] Chrostowski, Lukas, and Michael Hochberg. Silicon photonics design: from devices to systems. Cambridge University Press, 2015.