This is the accepted version of the following paper published by IEEE Transactions on Electron Devices:

H. Rahbardar Mojaver and P. Valizadeh, "Reverse Gate-Current of AlGaN/GaN HFETs: Evidence of Leakage at Mesa Sidewalls," in IEEE Transactions on Electron Devices, vol. 63, no. 4, pp. 1444-1449, April 2016.

doi: 10.1109/TED.2016.2529301

Reverse Gate-Current of AlGaN/GaN HFETs: Evidence of Leakage at Mesa Sidewalls

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***Abstract*— Reverse gate-current of AlGaN/GaN heterostructure field-effect transistor is studied over a wide range of lattice-temperatures from 150 to 490K. For gate-source voltages approaching zero volt signatures of gate-to-two dimensional electron gas leakage through the sidewalls of the mesa are observed. For exploring this leakage path a group of devices built on a number of alternative isolation-features of different geometries, and with different number of gate-covered sidewalls, are investigated. Among these devices which were realized on an identical layer structure (produced following the same fabrication technology with identical gate-length and -width), as the number of isolation-feature sidewalls overlapping with the gate-metal increases a rise in the gate-current is observed. The identified sidewall-leakage is not only consequential in devices built on isolation-feature geometries presenting more than two sidewalls, but it can also compete with mechanisms such as Poole-Frenkel, Fowler-Nordheim, and Trap-Assisted Tunneling which are traditionally considered in devices built on cubic mesas. In the present study relevance of these other transport mechanisms is also re-evaluated. It is observed that at temperatures below 320K among all of the explored devices sidewall leakage becomes more dominant than the Poole-Frenkel and Trap-Assisted Tunneling processes.**

***Index Terms*—AlGaN/GaN heterojunction field-effect transistor (HFET), gate leakage, isolation-feature geometry, sidewall leakage.**

I. Introduction

In spite of the larger Schottky barrier-height, reverse gate-current of AlGaN/GaN hetrostructure field-effect transistors (HFETs) has been so far observed to remain at higher levels compared to the AlGaAs/GaAs counterparts [1]-[3]. The higher leakage is usually attributed to the high density of traps residing within the AlGaN barrier [1]-[12]. Over the past two decades, a number of models relying on mechanisms such as multistep tunneling through the AlGaN barrier, also known as Trap-Assisted Tunneling (TAT) [1], [2], [4], and Poole-Frenkel (PF) leakage through a continuum of trap states in the barrier have been proposed [5]-[10]. These mechanisms are believed to be the dominant leakage processes for moderate values of temperature and gate-source bias.

In addition, gate-leakage in AlGaN/GaN HFETs has been sometimes observed to take a one step tunneling approach. When the electric-field across the barrier is strong enough, Fowler-Nordheim tunneling (FN) across the barrier is often detected [11], while when the electron-temperature is moderately elevated thermionic field-emission (TFE) takes over. There are also some studies on surface leakage in the form of hopping through surface traps from the gate to the source and drain contacts [12]. This current component can become significant at large gate-source or gate-drain biases.

Temperature- or bias-dependence of these leakage mechanisms can be used to distinguish between the aforementioned culprits. Since depending on a set of deterministic parameters (i.e. Schottky barrier-height, electric-field, and temperature), among these processes FN and TFE are easier to be recognized. However, due to the strong dependence on trap characteristics the choice of parameters used in TAT and PF is not as straightforward.

In the present work, temperature- and bias-dependent study of the gate-current in a group of devices built on alternative isolation-feature geometries is performed. Details of the fabrication process of these devices which offer a larger number of gate-covered sidewalls have been previously reported in [13]. For each isolation-feature geometry the gate-current studies reveal a correlation between the gate-current and the number of gate-covered sidewalls. Uncorrelated to the aforementioned leakage mechanisms, this observation provides evidence into the existence of a leakage path between the two-dimensional electron gas (2DEG) and the gate-metal. Although this has been already identified as a leakage path in Schottky test structures made on AlGaN/GaN epilayers [14], and also in a few transistors such as GaInP/InGaAs [15], and InAlAs/InGaAs HFETs [16], [17], its relevance to modeling the gate-leakage of AlGaN/GaN HFETs and its voltage and temperature dependence have attracted limited attention [18]-[20].

Section II presents the theoretical bases for modeling of reverse gate-current. Section III provides the discussion on the observed trends of temperature-, bias-, and geometry-dependence of the gate-current. This discussion is followed by the conclusion in section IV.

II. Theory

Figure 1 presents the typical thermal equilibrium conduction-band diagram of a polar AlGaN/GaN HFET under the gate electrode. On this figure, leakage paths according to the FN, TFE, PF, and TAT mechanisms are schematically highlighted.

Manuscript received October 1, 2015; revised December 3, 2015. This work was supported by the Natural Sciences and Engineering Research Council of Canada Discovery Grant Program. The authors are with the Department of Electrical and Computer Engineering, Concordia University, Montreal, QC H3G 1M8, Canada (e-mail: p.valizadeh@ieee.org).

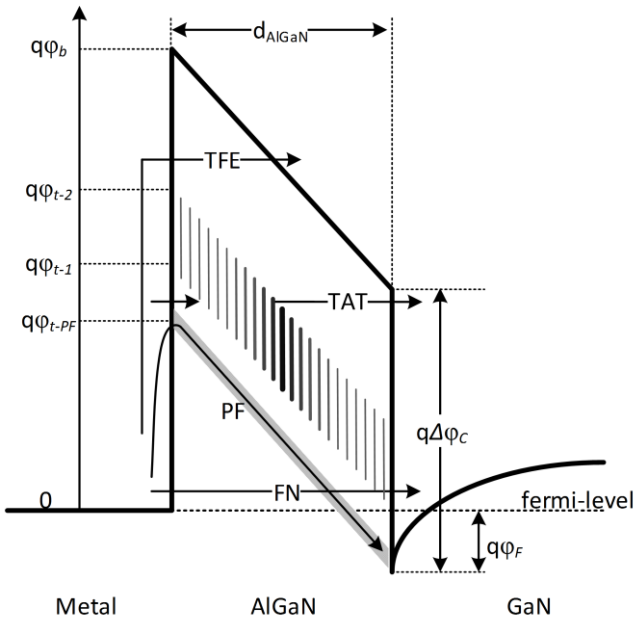

Fig. 1. Typical thermal equilibrium conduction-band diagram of a gated AlGaN/GaN HFET structure. Four major leakage mechanisms are schematically illustrated. FN and TFE are one-step tunneling processes taking place near the fermi level and at higher energy levels, respectively. PF is an emission transport through a continuum of trap states, while TAT is a two-step tunneling via scattered traps within the AlGaN barrier layer.

In presence of electric-field E across the barrier, electrons can tunnel through the AlGaN layer (from the metal fermi level to the conduction-band of GaN) via the FN tunneling process. According to this process, the current density is given by [1], [5],

$$J_{FN} = \frac{q^2 (m_0 / m_n^*)}{8\pi h \phi_b} E^2 \exp\left(- \frac{8\pi\sqrt{2m_n^* q}}{3hE} \phi_b^{3/2} \right) \quad (1)$$

in which q is the fundamental electronic charge, h is Planck constant, m_0 is the free-electron mass, m_n^* is the conduction-band effective mass in AlGaN, and $q\phi_b$ is the Schottky barrier-height (considering barrier-lowering caused by the presence of image-force and the thermal effect). Under the gate-source bias V_{GS}, according to the parameters identified in Fig. 1 the electric-field is given by,

$$E = \frac{\phi_b - V_{GS} - \Delta\phi_c + \phi_F}{d_{AlGaN}} \quad \text{for } V_{GS} > V_{th} \quad (2)$$

in which, d_{AlGaN} is the barrier thickness and V_{th} is the HFET's threshold-voltage.

The parameter ϕ_F can be determined precisely as a function of V_{GS} using variational method [21]. For specific value of barrier's aluminum mole fraction of 0.3 and d_{AlGaN} of 20 nm the following linear approximation is accordingly adopted:

$$\phi_F(V) = 0.32 - 0.08 \times V_{GS}. \quad (3)$$

Due to effective depletion of the 2DEG at gate-source biases lower than the threshold-voltage, the electric-field across the barrier becomes almost saturated in this range of bias.

Tunneling may also occur via TFE when thermally energized electrons rise to higher energy levels, from where they tunnel through the thinner physical barrier. Current density according to TFE is given by [1],

$$J_{TFE} = \frac{qA^*T}{k} \times \int_0^{\phi_b} \frac{1}{1+\exp[q(\phi_b - \phi)/kT]} \exp\left(- \frac{8\pi\sqrt{2m_n^* q}}{3hE} \phi_b^{3/2} \right) d\phi \quad (4)$$

in which, in addition to the aforementioned parameters T is the temperature in Kelvin, A^* is the Richardson constant, and k is the Boltzmann constant.

In case of carrier transport via traps, two main mechanisms are usually considered. One of these mechanisms is the PF electron emission from metal (or, a trap level in the barrier very close to the metal fermi level), into a continuum of states in the barrier associated with a conductive dislocation. It is through this continuum of states that electrons can directly transport to the GaN channel. The PF current density is accordingly explained by [5],

$$J_{PF} = C_{PF} E \exp\left(- \frac{q\left(\phi_{t-PF} - \sqrt{qE/\pi\varepsilon_0\varepsilon_s}\right)}{kT} \right) \quad (5)$$

in which, in addition to the aforementioned parameters ε_0 is the permittivity of free space, ε_s is the relative dielectric permittivity of AlGaN at high frequencies, $q\phi_t$ is the barrier-height for electron emission from the trap state, and C_{PF} is a constant.

The other trap-assisted transport mechanism is TAT in which electrons first tunnel from the gate-metal to a band of localized traps in the barrier, followed by tunneling to the GaN channel. Current density according to this process can be expressed by [1],

$$J_{TAT} = \frac{q}{E} \int_0^{\phi_{t-2}} \left(1/R_1 + 1/R_2 \right)^{-1} d\phi \quad (6)$$

TABLE I
VALUES OF THE PARAMETERS USED IN (1)-(6)

Sym.	Value	Unit	Ref.
m_n^*	$0.22\times9.11\times10^{-31}$	kg	[22]
ϕ_b	$1.15 - 4.7\times10^{-6}\sqrt{E}$	V	[1], [22]
A^*	2.73×10^{-5}	$Am^{-2}K^{-2}$	[1]
C_{PF}	10^{-9}	$Am^{-1}V^{-1}$	[3]
ε_s	5.1	---	[5]
ϕ_{t_PF}	0.3	V	[5]
ϕ_{t_1}	0.45	V	[1]
ϕ_{t_2}	1.11	V	[1]
N_t	1.5×10^{13}	cm^{-3}	[1]
$\Delta\phi_c$	0.42	V	[22]

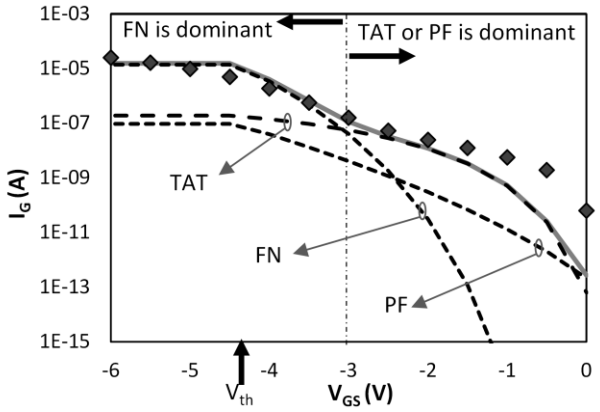

Fig. 2. PF, FN, and TAT leakage components as functions of V_{GS}. The continuous gray curve is the sum of the three components. The room-temperature experimental data points are presented by the diamond marks. V_{DS} is equal to zero volt.

in which R_1 and R_2 represent tunneling rates from metal to the lower edge of the localized trap band and from the higher edge of the trap band to 2DEG, respectively. According to Karmalkar *et al.*, R_1 and R_2 are determined as functions of E, $q\phi_{t-1}$, $q\phi_{t-2}$, and N_t [1], where $q\phi_{t-1,2}$ are identified in Fig. 1 and N_t represents the trap density. Considering (6), traps located near the middle of the barrier have the highest probability of contribution to TAT. This is since one of the two tunneling probabilities dramatically reduces for the traps located in the vicinity of the surface, or the interface.

On the basis of the theory presented in (1)-(6), it has been attempted to demonstrate the predicting power of each of the four aforementioned leakage mechanisms in case of the room-temperature gate-current of an $Al_{0.3}Ga_{0.7}N$/GaN HFET of 20 nm barrier thickness, when biased at V_{DS}=0 V for multiple negative values of V_{GS}. This device was fabricated on a cubic mesa, imposing only two gate-covered sidewalls. The fabrication process of this device which has a gate-length of 0.5 μm and gate-width of 100 μm has been previously reported in [13]. The threshold-voltage (V_{th}) of this transistor is equal to -4.5 V. Table I presents the values of the parameters used in calculation of the leakage-current according to each mechanism. These values are picked in an attempt to behaviorally predict the responsible mechanism for the experimentally observed gate-leakage with the variation of V_{GS}. Accordingly, Fig. 2 depicts the V_{GS}-dependence of three of the previously mentioned leakage-components, while due to the low temperature of measurement TFE was not consequential.

The typically observed gate-leakage behavior presented in Fig. 2 illustrates the presence of a turning point before V_{GS} becomes as negative as the threshold-voltage. For values of V_{GS} less negative than this turning point, since according to (1) and (2) the FN process is dramatically less likely, the gate-current can be only explained by the trap-related processes of PF and TAT. However, beyond this turning point the increase and eventual saturation of E gives the FN process the dominant role.

As shown in Fig. 2, even without attempting to get a best fit to the experimental data, adopting the typical values of the parameters used by others in modeling the gate-leakage of similar devices provides an acceptable level of matching to the gate-current of this transistor. This is with the exception of V_{GS} values close to zero volt. In which case, the evidence provided in section III identifies another dominant mechanism of leakage.

In the calculations presented in this section determining E and ϕ_b follow an iterative approach, as E and ϕ_b are mutually dependent. In the first iteration ϕ_b is calculated assuming zero electric-field, followed by the recalculation of E. This procedure continues until convergence.

It should be mentioned that the discussed leakage components are those which are responsible for leakage from gate to the 2DEG, hence excluding surface leakage. This is in agreement with the choice of V_{DS} = 0 V and moderate values for V_{GS}.

III. Results and Discussion

In an attempt to investigate the contributions of the gate-covered mesa-sidewalls to the gate-current of AlGaN/GaN HFETs, the V_{GS}-dependence of this current component is studied across a number of devices built on a few alternative isolation-features (instead of the regular cubic mesa). The structures of these devices are depicted in Fig. 3. All these devices were built on an epitaxial layer structure consisting of a 20 nm thick unintentionally doped (UID) $Al_{0.3}Ga_{0.7}N$ barrier, a 1 nm thick AlN spacer, and a UID GaN channel followed by the Fe-doped GaN buffer layer. Further details of the fabrication process have been previously reported [13]. Figure 4 provides gate-dissected cross-sectional views of the fin, 7-island, and 14-island device varieties with indication of the size of the important dimensions. Based on the structures presented in Fig. 3, since the likewise defined cross-sectional views are identical in case of the 14-island, comb, ladder, and inverted-fin structures, the 14-island is taken as a representative. As shown in Fig. 4, all of the investigated transistors share an almost equal value of gate-width.

Figure 5 provides plots of the room-temperature measured I_G for the transistors depicted in Fig. 3. Among these plots, as theoretically presented in section II for large negative values of V_{GS}, FN is deemed the dominant leakage process (FN regime). In this regime, all of the devices demonstrate approximately equal values of gate-current. For less negative values of V_{GS} disappearance of this observation among the devices having unequal number of gate-overlaps with the 2DEG at the sidewalls of the isolation-feature heralds the beginning of a FN-unrelated regime (excess-leakage regime). As observed on this figure, the gate-current among the 14-island, ladder, comb, and the inverted-fin structures remains identical even under the excess-leakage regime. However, the gate of the 7-island and fin-isolated devices demonstrate more than one order of magnitude less leakage than these groups of devices. Based on the almost equal values of the effective gate-width among all of the aforementioned transistor varieties (from 98 to 100 μm), the sizeable difference between the

values of I_G identifies a leakage path unrelated to the size of the gate-overlapped top surface of the isolation-feature. Hence, the excess leakage is expected to be unrelated to FN-, PF-, and TAT-governed leakage through the AlGaN barrier in a path normal to the heterointerface.

A seemingly responsible explanation for this observation can be sought in the difference between the surface components of gate-leakage when the transistor is realized on an isolation-feature with a footprint wider than the effective gate-width. However, considering the fact that the isolation-feature height is only 300 nm, this explanation is deemed incapable of yielding an answer to the orders of magnitude difference in I_G. This is since the difference in the overall surface area at the source and drain access-regions among all devices varieties is considerably smaller. This argument is further supported by the similarity of the gate-leakage among the ladder and 14-island device varieties. According to Fig. 3, among these two groups although the latter presents drain and source access-regions on the sidewalls of the features and on the etched GaN surface, in the former group such regions are only formed on the AlGaN surface. The explanation based on the variation of the surface-component of gate-leakage is even

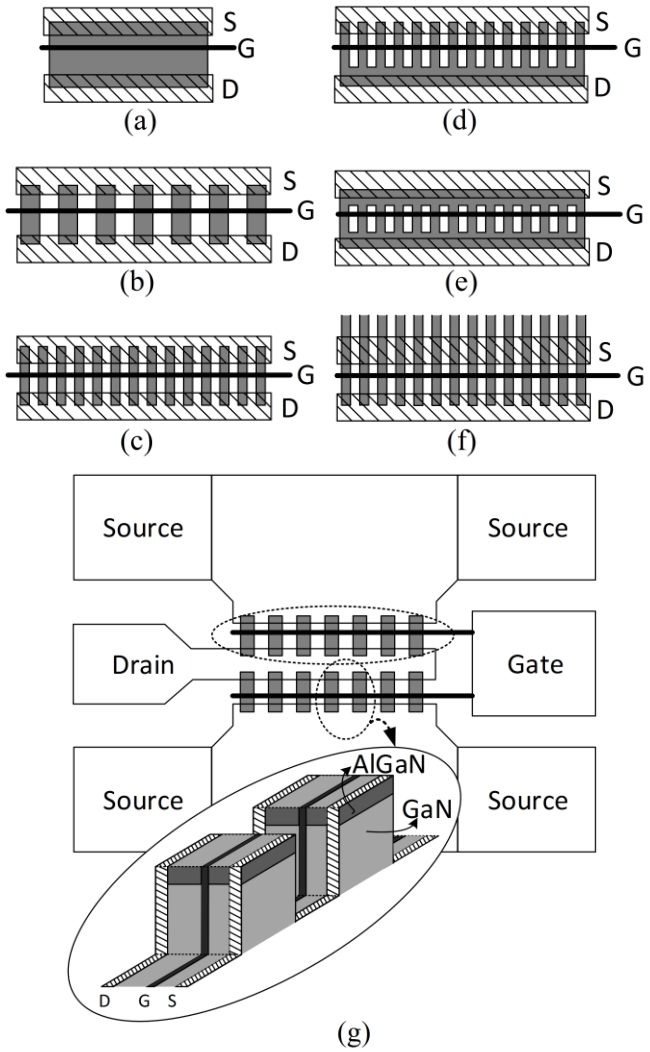

Fig. 3. (a)-(f) represent the top views of devices built on isolation-features known as: fin, 7-island, 14-island, comb, ladder, and inverted-fin, respectively. In case of the inverted-fin, only the widths of the fins within the proximity of one gate finger are shown. The gray areas on these top views represent the surface of each isolation-feature resulting from etching of the AlGaN/AlN/GaN structure to a 300 nm depth. The aforementioned names are illustrative of these shapes. Among these figures, the hash-marked areas represent the ohmic contact of source and drain, and the black lines stand for gate-fingers. (g) represents the complete top view of a two-finger HFET with the depiction of contact pads in case of the 7-island structure represented in (b).The inset shows the 3D schematic in case of two of the islands. The area marked by the larger oval is the area presented in (b).

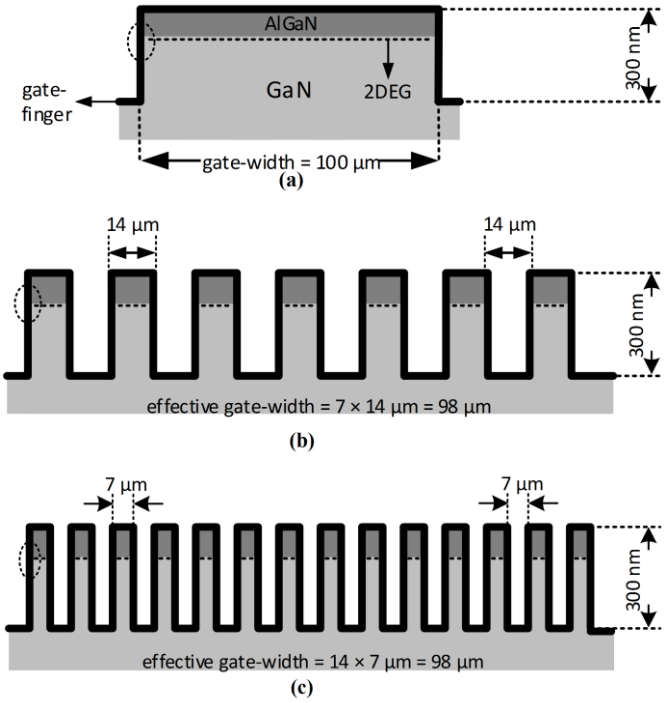

Fig. 4. Gate-dissected cross-sectional views of the fin (a), 7-island (b), and 14-island (c) device varieties with indication of the size of the important dimensions. The cross-sectional views are provided in planes parallel with the gate-finger. The heights of the features are not drawn to scale. The color code of the layer structure expressed in (a) is also applicable to (b) and (c). In each case, as an example on one of the gate-covered sidewalls the point of overlap of the gate-finger and the 2DEG is identified by the dashed oval.

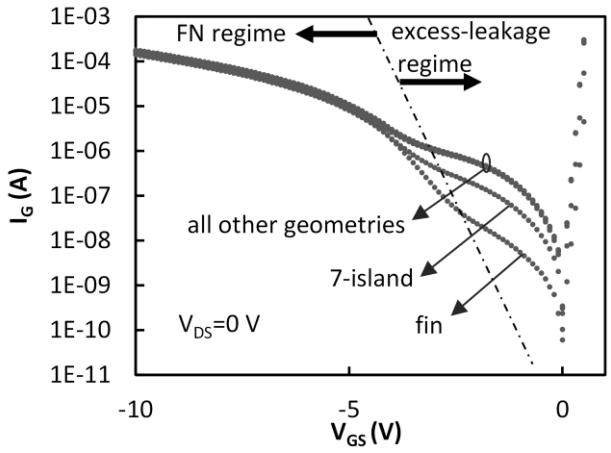

Fig. 5. Measured I_G versus V_{GS} for the devices built on the six different isolation-feature geometries presented in Fig. 3. The lowest and the middle curves are associated with fin and 7-island isolation-feature geometries, respectively. Curves for 14-island, comb, ladder, and inverted-fin which all consist of 14 individual features interfacing the gate-finger exactly coincide with one another. Measurements were performed at room temperature.

less likely to hold when considering the fact that all exposed surfaces of these devices were passivated with a SiN_x film, which has been reported to reduce the surface leakage at least by two orders of magnitude [23]. Success of the surface passivation process was assessed by the lack of observation of gate-lag, and frequency dispersion on drain-current and gate-transconductance of all device varieties.

The remaining explanation for the observations made on Fig. 5 is provided in terms of the presence of a leakage path between the gate-metal and the 2DEG where the gate is touching the etched sidewall of the isolation-feature. For a wide range of temperatures (150 to 490K), Fig. 6 presents the recorded values of I_G under the FN – and the excess-leakage regimes. The samples were placed in the temperature-controlled chamber of a MMR-LTMP4 probe station. This probe station can reliably maintain the lattice temperature at any temperature between 80 and 500K. During measurements, the probe station chamber was operated under low pressure (i.e., less than 1 mTorr) and the chamber temperature was controlled and monitored by a temperature controller (MMR-K20).

Since sidewall leakage from gate metal to 2DEG depends on 2DEG characteristics such as the 2DEG concentration, for a fair assessment amongst these devices the previously reported correlation between the geometry of the isolation-feature and the threshold-voltage is appreciated through biasing the devices at identical values of the effective gate-source voltage ($V_{GS\text{-}eff} = V_{GS} - V_{th}$), instead of identical values of V_{GS} [13]. The threshold-voltage V_{th} is equal to -4.4, -4.3, and -4 V for fin, 7-island, and 14-island device varieties, respectively. In the data presented in Fig. 6, values of $V_{GS\text{-}eff}$ in the excess-leakage and FN regimes are selected equal to 3 and -6 V, respectively.

According to the data presented in Fig. 6 and supporting the observation made on Fig. 5, where the FN is dominant very little difference among the gate-currents of the explored transistors is observed. In spite of the absence of T in (1), the slight temperature-dependence observed under this regime is owing to the effect of thermal barrier-lowering. However, under the excess-leakage regime the transistor offering the lowest number of sidewalls interfacing the gate-finger (fin-isolated) shows the lowest value of the gate-current. Among the explored devices, the gate-current is observed to increase when the number of gate-covered sidewalls increases to 14 and eventually 28. Considering the I_G to be composed of two components defined in terms of I_1 and I_2, where I_1 is representing the through-barrier gate-leakage normal to the surface of the heterostructure and I_2 is standing for the sidewall leakage from the gate metal to the 2DEG on one sidewall, between these three groups of data I_G is supposed to be equal to I_1+2I_2, I_1+14I_2, and I_1+28I_2, respectively. Based on the first two expressions values of I_1 and I_2 were calculated for all of the measurement temperatures. As shown in Fig. 6, employing these values is observed to provide an excellent level of matching to the groups of devices presenting 28 sidewall overlaps with the gate-finger. While at temperatures below 320K , I_2 expresses a larger share of the gate-current, I_1 becomes more important at higher temperatures. This observation clearly highlights the importance of the gate-to-2DEG leakage at the sidewalls at low temperatures and even at temperatures higher than 320K when the number of sidewalls is large. This is since I_2 should be multiplied by the number of sidewalls to be compared to I_1.

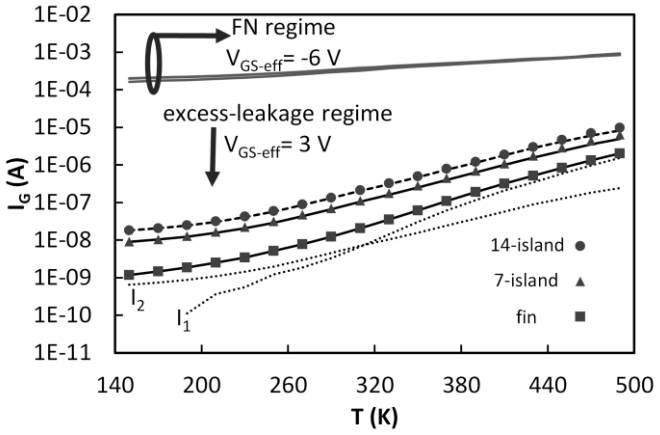

Fig. 6. Representative temperature-dependent gate-current of fin, 7-island, and 14-island isolated HFETs. Measurements are performed at $V_{GS\text{-}Eff}$ = -6 V (FN regime) and $V_{GS\text{-}eff}$ = 3 V (excess-leakage regime), where in both cases V_{DS} = 0 V. The dashed curve presents the expected values of I_G calculated for the 14-island isolated HFET based on the recorded I_G of the fin- and the 7-island isolated devices. Symbols represent experimentally acquired data points. Curves marked by I_1 and I_2 stand for the calculated components of the gate current through the AlGaN barrier and leakage to the 2DEG at one sidewall, respectively. For clarity of presentation, the symbols are not shown in the FN regime.

These observations substantiate the speculation of the gate-to-2DEG leakage as the mechanism of excess leakage among the devices presenting larger number of gate-covered isolation-feature sidewalls.

IV. Conclusion

Reverse gate-current of AlGaN/GaN HFET was investigated for a group of devices built on a number of alternative isolation-features of different geometries. Results revealed evidences on the presence of a leakage path at the sidewalls of the isolation-feature between the gate-metal and the 2DEG. It was observed that this leakage current increases with the number of isolation-feature sidewalls overlapping with the gate-metal and eventually becomes proportional to it at low to moderate temperatures.

References

[1] S. Karmalkar, D. M. Sathaiya, and M. S. Shur, "Mechanism of the reverse gate leakage in AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 82, no. 22, pp. 3976-3978, June 2003.

[2] S. Sudharsanan and S. Karmalkar, "Modeling of the reverse gate leakage in AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 107, no. 6, pp. 064501-1–064501-3, Mar. 2010.

[3] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta, and N. DasGupta, "Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling," *IEEE Trans. Electron Dev.*, vol. 60, no. 10, pp. 3157-3165, Oct. 2013.

[4] R. Jos, "Reverse Schottky gate current in AlGaN-GaN high-electron-mobility-transistors," *J. Appl. Phys.*, vol. 112, no. 9, pp. 094508-1–094508-7, Nov. 2012.

[5] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 99, no. 2, pp. 023703-1–023703-6, Jan. 2006.

[6] E. J. Miller, E. T. Yu, P. Waltereit, and J. S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 535-537, Jan. 2004.

[7] O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," *J. Appl. Phys.*, vol. 95, no. 11, pp. 6414-6419, June 2004.

[8] S. Ganguly, A. Konar, Z. Hu, H. Xing, and D. Jena, "Polarization effects on gate leakage in InAlN/AlN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 101, no. 25, pp. 253519-1–253519-5, Dec. 2012.

[9] D. Yan, H. Lu, D. Cao, D. Chen, R. Zhang, and Y. Zheng, "On the reverse gate leakage current of AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 97, no. 15 , pp 153503-1–153503-3, Oct. 2010.

[10] S. Ghosh, A. Dasgupta, S. Khandelwal, S. Agnihotri, and Y. S. Chauhan "Surface-potential-based compact modeling of gate current in AlGaN/GaN HEMTs," *IEEE Trans. Electron Dev.*, vol. 62, no. 2, pp. 443-448, Feb. 2015.

[11] S. Turuvekere, D. S. Rawal, A. DasGupta, and N. DasGupta. "Evidence of Fowler–Nordheim Tunneling in Gate Leakage Current of AlGaN/GaN HEMTs at Room Temperature," *IEEE Trans. Electron Dev.*, vol. 61, no. 12, pp. 4291-4294, Dec. 2014.

[12] J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, "Mechanism of surface conduction in the vicinity of Schottky gates on AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 91, no. 9, pp. 093501-1–093501-3, Aug. 2007.

[13] A. Loghmany and P. Valizadeh, "Alternative isolation-feature geometries and polarization-engineering of polar AlGaN/GaN HFETs," *Solid-State Electron.*, vol. 103, pp. 162-166, Aug. 2014.

[14] C. Xu, J. Wang, H. Chen, F. Xu, Z. Dong, Y. Hao, and C. P. Wen. "The leakage current of the Schottky contact on the mesa edge of AlGaN/GaN heterostructure," *Electron Dev. Lett.*, vol. 28, no. 11, pp. 942-944, Nov. 2007.

[15] W. L. Chang, H. J. Pan, W. C. Wang, K. B. Thei, W. S. Lour, and W. C. Liu., "Influences of the mesa-sidewall effect on $Ga_{0.51}In_{0.49}P/In_{0.15}Ga_{0.85}As$ pseudomorphic transistors," *Semicond. Sci. Technol.*, vol. 14, no.10, pp. 887-891, July 1999.

[16] S. R. Bahl and J. A. del Alamo, "Elimination of Mesa-Sidewall Gate Leakage in InAlAs /InGaAs Heterostructures by Selective Sidewall Recessing," *IEEE Trans. Electron Dev.*, vol. 13, no. 4, pp. 195-197, Apr. 1992.

[17] A. S. Brown, C. S. Chou, M. J. Delaney, C. E. Hooper, J. F. Jensen, L. E. Larson, U. K. Mishra, L. D. Nguyen, and M. S. Thompson. "Low-temperature buffer AlInAs/GaInAs on InP HEMT technology for ultra-high-speed integrated circuits," *proceedings of GaAs IC. Symp.*, pp. 143-146, 1989.

[18] Y. S. Lin, Y. W. Lain, and S. S. Hsu, "AlGaN/GaN HEMTs with low leakage current and high on/off current ratio," *Electron Dev. Lett.*, vol. 31, no. 2, pp. 102-104, Feb. 2010.

[19] J. Kováč, A. Šatka, A. Chvála, D. Donoval, P. Kordoš, and S. Delage, "Gate leakage current in GaN-based mesa-and planar-type heterostructure field-effect transistors," *Microelectronics Reliability*, vol. 52, no. 7, pp. 1323-1327, Feb. 2012.

[20] P. Liu, C. Xie, F. Zhang, J. Chen, and D. Chen, "Elimination of gate leakage in GaN FETs by placing oxide spacers on the mesa sidewalls," *Electron Dev. Lett.*, vol. 34, no. 10, pp. 1232-1234, Oct 2013.

[21] F. Manouchehri, P. Valizadeh, and M. Z. Kabir, "Determination of subband energies and 2DEG characteristics of $Al_xGa_{1-x}N$/GaN heterojunctions using variational method," *J. Vac. Sci. Technol. A*, vol. 32, no. 2, pp. 021104-1–021104-8, Mar. 2014.

[22] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 11, pp. 3222-3233, Mar. 1999.

[23] [19] Y. H. Chen, K. Zhang, M. Y. Cao, S. L. Zhao, J. C. Zhang, X. H. Ma, and Y. Hao, "Study of surface leakage current of AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 104, no. 15, pp. 153509-1–153509-4, Apr. 2014.