Fabrication and Physics-Based Modeling of Polar AlGaN/GaN and AlInGaN/GaN HFETs

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ABSTRACT

Fabrication and Physics-Based Modeling of Polar AlGaN/GaN and AlInGaN/GaN HFETs

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Since their advent, polar AlGaN/GaN hetero-junction field effect transistors (HFETs) have drawn a great deal of attention especially in high frequency/high power applications. However, the superb prospects of these transistors are affected by a few drawbacks such as aging/crack formation under strain, presence of high gate-leakage, and challenging realization of enhancement-mode (normally-off) devices.

Quite recently, study of quaternary AlInGaN barriers has been presented as a promising avenue for fulfilling various design demands including: lattice matching, polarization matching, and positive shifting the inherently negative threshold voltage of AlGaN/GaN HFETs. However, thus far only a limited scope of theoretical studies on AlInGaN/GaN hetero-structure characteristics has been reported. As part of this thesis, the two dimensional electron gas (2DEG) characteristics of gated metal-face wurtzite AlInGaN/GaN hetero-junctions as function of physical and compositional properties of the hetero-junction are theoretically evaluated using the variational method. According to this study, a considerable shift in the positive direction for the threshold voltage of AlInGaN/GaN HFETs can be achieved by engineering both the spontaneous and the piezoelectric polarization (using a quaternary AlInGaN barrier-layer of appropriate mole-fractions). Succeeding this study, a novel quaternary lattice-match layer structure based on employing a bilayer barrier for improving the carrier confinement in the channel of

enhancement-mode AlInGaN/GaN HFETs is for the first time proposed. It is shown that while the proposed layer structure substantially improves the carrier confinement in the GaN channel layer, it also upholds the merits of employing a lattice-match barrier towards achieving an enhancement-mode operation.

One of the most important device characteristics of AlGaN/GaN HFETs which is often poorly understood is the gate-leakage current. As part of this thesis, reverse gate-leakage of AlGaN/GaN HFETs is studied over a wide range of lattice-temperatures. While unveiling an obscure path for gate leakage through the mesa sidewall, a model considering different leakage paths, including the identified sidewall leakage, is presented. It is illustrated that the sidewall path to the 2DEG is associated with the Poole-Frenkel electron emission. The novel contribution of the present analysis is that it postulates that in absence of absolute uniformity, Fowler-Nordheim (FN) tunneling takes place through only a small portion of the surface of the barrier, which boasts the highest electric field or the smallest Schottky barrier height. This consideration, allows the model to avoid unrealistic values for quantities such as effective electron mass (that has plagued many of the existing models).

Also as part of this thesis work, process recipe for microfabrication of submicron gate AlGaN/GaN HFETs using electron beam lithography was developed at McGill's nano-tools micro-fabrication facilities. The results of DC characterization of the fabricated transistors along with the results of the DC stress test are presented.

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I would like to express my deep gratitude to my supervisor, Dr. Pouya Valizadeh, for imparting his knowledge and expertise in this thesis. This work would not have been completed without his guidance, persistent help, and enduring support. I am also very grateful to the members of the examining committee Dr. T. Paul Chow, Dr. A. Ben Hamza, Dr. Mojtaba Kahrizi, and Dr. M. Zhahangir Kabir, for their valuable time to review my thesis and also their useful comments.

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Contents

List of Figures

List of Tables

List of Symbols

Symbol	Description	Unit (SI)
x	Aluminum mole fraction	---
y	Indium mole fraction	---
P_{PZ}	Piezoelectric polarization	C/m^2
P_{SP}	Spontaneous polarization	C/m^2
μ	Basal strain	---
b_{sp}^{AlGaN}	Ternary AlGaN bowing parameter for spontaneous polarization	C/m^2
b_{sp}^{InGaN}	Ternary InGaN bowing parameter for spontaneous polarization	C/m^2
b_{sp}^{AlInN}	Ternary AlInN bowing parameter for spontaneous polarization	C/m^2
b_{EG}^{AlGaN}	Ternary AlGaN bowing parameter for the band gap	J
b_{EG}^{InGaN}	Ternary InGaN bowing parameter for the band gap	J
b_{EG}^{AlInN}	Ternary AlInN bowing parameter for the band gap	J
σ	Polarization-induced sheet charge density	C/m^2
$q\phi_b$	Schottky barrier height	J
$q\phi_m$	Metal work function	J
$q\phi_t$	Barrier height for the electron emission from the trap state at the mesa sidewall	J
$q\phi_F$	Difference between fermi energy level and conduction-band edge at the GaN side in AlGaN/GaN HFETs	J
$q\chi$	Electron affinity	J
ϵ	Permittivity	F/m
ϵ_0	Vacuum permittivity	F/m

ϵ_r	Relative low frequency permittivity	---
ϵ_s	Relative high frequency permittivity	---
$d_{AlInGaN}$	Thickness of AlInGaN barrier layer	m
d_{AlGaN}	Thickness of AlGaN barrier layer	m
ΔE_C	Conduction-band offset	J
E	Electric field	V/m
V_G	Gate voltage	V
V_{GS}	Gate-source voltage	V
V_{DS}	Drain-source voltage	V
I_G	Gate current	A
J_G	Gate current density	A/m^2
J_{FN}	Fowler-Nordheim current density	A/m^2
J_{PF}	Poole-Frenkel current density	A/m^2
I_D	Drain current	A
n_s	2DEG electron concentration	m^{-2}
n_{s_GaN}	Electron concentration in GaN	m^{-3}
n_{s_AlGaN}	Electron concentration in barrier	m^{-3}
n_{s_total}	Total electron concentration	m^{-3}
E_0	Energy level of the first subband energy level	J
E_1	Energy level of the second subband energy level	J
D_S	Two dimensional density of states	s^2/m^4kg
z	Distance from the gate-metal/barrier Schottky contact	m

V_{th}	Threshold voltage	V
ψ_n	Wavefunction of the (n-1)th subband	---
q	Elementary charge	C
E_F	Fermi energy level	J
E_G	Bandgap energy	J
k	Boltzmann constant	J/K
T	Temperature	K
m_0	Free electron mass	Kg
m^*	Electron effective mass	Kg
α	Varshni empirical constant	J/K
β	Constant defined in close association with the Debye Temperature	K
γ	Magnification of electric field across the Fowler-Nordheim leakage zone	---
S_{FN}	Fowler-Nordheim leaking zone area	m^2
C_{PF}	Poole-Frenkel proportional constant	---
$E_{sidewall}$	Electric field defined in terms of the potential difference between gate and the 2DEG	V/m
m_{PF}	Proportionality factor related to the electric field at the mesa sidewall	---
D	Exposure area dose for e-beam lithography	C/m^2
I_B	Electron beam current	A
cc	Center to center spacing	m
L_s	Line spacing	m
$Dwell$	Exposure time for each point	s
SS	Subthreshold swing	V/dec

List of Abbreviations

Abbreviation	Description
2DEG	Two dimensional electron gas
EBL	Electron beam lithography
HFET	Hetero-junction field effect transistor
TAT	Trap-assisted-tunneling
PF	Poole-Frenkel
FN	Fowler-Nordheim
TFE	Thermionic field emission
UID	Unintentionally doped
SEM	Scanning electron microscope
NPGS	Nanometer pattern generation system
UV	Ultra violet
IPA	Isopropyl alcohol
DI water	Deionized water
sccm	Standard cubic centimeter per minuet
MERIE	Magnetically-enhanced reactive ion etching
RTA	Rapid thermal annealing

Chapter 1

Introduction

1.1 Overview of III-nitride technology

Over the last two decades, wide-bandgap materials, such as GaN, SiC, AlN, and BN have attracted a great deal of attention for fulfilling the growing demands in high-power mm-wave and high-voltage power-electronic applications [1], [2]. Among them, GaN shows excellent device/material properties, including large sheet carrier concentration in AlGaN/GaN hetero-junction (i.e., in the order of 10^{13} cm^{-2}) and high breakdown field (i.e., about 4 MV/cm). As a result of these properties, GaN transistors have demonstrated a record of 6.7 W/mm power density with an associated power-added efficiency of 14.4% at 94 GHz[3], f_T/f_{max} of 454/444 GHz [4], current densities in excess of 1 A/mm, and

breakdown voltages exceeding 2000 V [5]. GaN power transistors rated up to 650 V are currently commercially available [6].

Notwithstanding these remarkable properties, III-nitride technology has faced a few problems such as lack of an affordable/large-size free-standing substrate, possibility of acquiring efficient p-type doping, presence of high gate-leakage in GaN-channel hetero-junction field effect transistors (HFETs), and challenging realization of enhancement-mode HFETs. Among these, the last two items highlight the major objectives of the present PhD research. Since this research is mainly focused on AlGaN/GaN HFETs, a very brief review of the fundamentals of these devices is presented in the next section.

1.2 AlGaN/GaN hetero-junction field effect transistors

Polar $Al_xGa_{1-x}N$/GaN hetero-junctions are formed by the pseudomorphic growth of a wider bandgap barrier-layer (i.e., $Al_xGa_{1-x}N$) on top of a narrower bandgap channel/buffer-layer (i.e., GaN). Due to the difference between the energy bandgaps of the barrier- and buffer-layer, a quantum well is generated in the channel/buffer side of the $Al_xGa_{1-x}N$/GaN hetero-junctions.

In the so-called polar wurtzite $Al_xGa_{1-x}N$/GaN hetero-junctions, the quantum well specifications in addition to bandgap discontinuity, and doping levels, are affected by the piezoelectric and spontaneous polarization fields (P_{SP} and P_{SP}, respectively).

The lattice mismatch between GaN and $Al_xGa_{1-x}N$ layers, coupled with the large piezoelectric coefficients among III-nitrides generates the piezoelectric polarization effect at the hetero-interface of pseudomorphically grown $Al_xGa_{1-x}N$/GaN hetero-structures. In addition to the piezoelectric polarization, there is a sizable discontinuity among the spontaneous polarization of wurtzite III-nitrides forming the hetero-junction. The strongest

spontaneous polarization among III-nitrides, which is observed in AlN, is only about 3–5 times smaller than that of typical ferroelectric perovskites [7]. Owing to both spontaneous and piezoelectric polarization effect, a high concentration two dimensional electron gas (2DEG) is induced at the GaN side of the metal-face AlGaN/GaN hetero-junctions [8]. The high concentration polar 2DEG typically induces a normally-on mode of operation among these devices.

By realizing the drain and source ohmic contacts to the 2DEG, as well as a Schottky contact made to the AlGaN barrier layer an HFET is realized. Figure 1.1 presents a cross-sectional view of a typical polar AlGaN/GaN HFET along with the artictic depiction of conduction-band diagram of the AlGaN/GaN hetero-junction.

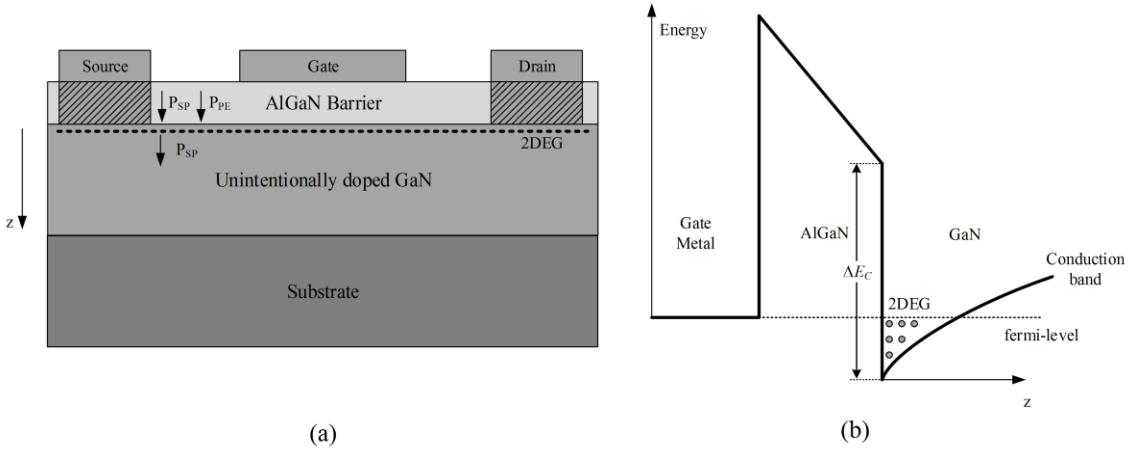

Figure 1.1 (a) Cross-sectional view of a typical polar AlGaN/GaN HFET. (b) The artistic depiction of the thermal-equilibrium conduction-band diagram of the AlGaN/GaN hetero-structure.

1.3 Research motivation

1.3.1 Motivation of study of gate leakage in AlGaN/GaN HFETs

In spite of the larger Schottky barrier-height, gate-current of AlGaN/GaN HFETs has been so far observed to be at higher levels compared to the AlGaAs/GaAs counterparts [9]-[11].

The higher than expected leakage is usually attributed to the high density of traps residing within the AlGaN barrier [9]-[20].

There are several leakage mechanisms which have been so far considered relevant to the gate-leakage of AlGaN/GaN HFETs. Most of these mechanisms are based on direct tunneling, or tunneling via traps, from the gate-metal to the 2DEG through the AlGaN barrier. Temperature- or bias-dependence of these different leakage mechanisms can be used to distinguish between them. Since depending on a set of deterministic parameters (i.e. Schottky barrier-height, electric-field, and temperature), among these processes direct tunneling mechanism is easier to be recognized. However, due to the strong dependence on trap characteristics, the choice of parameters used in tunneling via traps is not as straightforward. This issue has caused a certain degree of ambiguity in understanding the underlying physics of gate leakage, and devising strategies for control it.

1.3.2 Motivation of study of quaternary $Al_xIn_yGa_{1-x-y}N$/GaN HFETs

Recently, in order to alleviate the problem of trap formation associated with strained epitaxy, employing lattice match $Al_{0.83}In_{0.17}N$/GaN hetero-structures in realization of HFETs has gained traction [21]. However, in these devices larger spontaneous polarization results in higher 2DEG density. This factor makes the depletion of 2DEG more difficult and as a result the threshold voltage more negative. Consequently, the realization of the attractive enhancement mode devices becomes even more difficult than in the traditional AlGaN/GaN technology.

Towards alleviating this problem, quaternary $Al_xIn_yGa_{1-x-y}N$/GaN HFETs can take advantage of the positive features of both AlInN/GaN and AlGaN/GaN hetero-structures

via providing an additional degree of freedom to the device design [22]. Through concurrent engineering of the Al and the In mole fraction, bandgap and polarization of the barrier can be tuned with more freedom. Based on this strategy, increasing the In mole fraction in $Al_xIn_yGa_{1-x-y}N$/GaN hetero-structure can reduce the polarization and eventually provide a true enhancement mode GaN-channel HFET.

1.3.3 Motivation for studying the fabrication recipes for submicron-gate GaN-channel HFETs

The previous efforts in the area of III-nitride micro-fabrication in the Reliable Electron Devices research group at Concordia University were limited by the confines of optical-lithography. In order to enhance the DC and RF characteristics of the studied HFETs, shrinking some of feature sizes of the device to sub-micron dimensions is inevitable. This explains the urgency for working on the newly established electron-beam lithography facility at McGill's nano-tools microfabrication facilities to replace the mode of lithography. Since every microfabrication facility, according to its existing equipment and available chemicals, uses a unique process recipe for the microfabrication, developing an in-house fabrication process for realization of sub-micron gate III-nitride HFETs is desired.

1.4 Research objectives

In accordance with the research motivations presented in section 1.3, the objectives of this PhD research were divided into three major categories. Devising a realistic physics-based model for the gate leakage, as an important concern in the operation of III-nitride HFETs, was the first objective of this PhD research. The second objective was to formulate a

theoretical variational model for 2DEG characteristics of AlInGaN/GaN quaternary HFETs and realistic assessment of those hetero-structures for yielding enhancement-mode GaN channel HFETs of sufficient degree of carrier confinement. The last objective was to develop the fabrication process for realization of sub-micron gate AlGaN/GaN and by extension AlInGaN/GaN HFETs.

1.5 Thesis layout

This thesis consists of five chapters. Following the introduction in chapter one, theoretical modeling of 2DEG characteristics of AlInGaN/GaN HFETs is presented in chapter 2. Extending from this work, chapter 3 proposes a novel bilayer lattice-match AlInGaN barrier structure for improving the channel carrier confinement of enhancement-mode AlInGaN/GaN HFETs. Modeling of gate-leakage in AlGaN/GaN HFETs, considering different leakage paths and electron transport mechanisms, is presented in chapter 4. Chapter 5 is dedicated to developing a fabrication process for realization of sub-micron gate AlGaN/GaN and by extension AlInGaN/GaN HFETs. Chapter 6 presents the concluding remarks on the contributions of this thesis, as well as suggested future works.

1.6 List of publications

The research work of this thesis has resulted in the following publications,

- H. R. Mojaver and P. Valizadeh, "Reverse gate-current of AlGaN/GaN HFETs: Evidence of leakage at mesa sidewalls," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1444-1449, Apr. 2016.
- H. R. Mojaver, F. Manouchehri, and P. Valizadeh, "Theoretical evaluation of two dimensional electron gas characteristics of quaternary $Al_xIn_yGa_{1-x-y}N$/GaN hetero-junctions," *J. Appl. Phys.*, vol. 119, no. 15, pp. 154502-1–154502-7, Apr. 2016.

- H. R. Mojaver, J. L. Gosselin, and P. Valizadeh, "Use of a bilayer lattice-matched AlInGaN barrier for improving the channel carrier confinement of enhancement-mode AlInGaN/GaN hetero-structure field-effect transistors," *J. Appl. Phys.*, vol. 121, no. 24, pp. 244502-1–244502-6, June 2017.

In addition, the following manuscript is currently under review:

H. R. Mojaver and P. Valizadeh, "Modeling the Reverse Gate-Leakage Current in GaN-Channel HFETs: Realistic Assessment of Fowler-Nordheim and Leakage at Mesa Sidewalls," submitted to *IEEE Trans. Electron Devices*, Feb. 2018.

Chapter 2

Theoretical modeling of 2DEG characteristics of AlInGaN/GaN HFETs

The contributions of this chapter have been already published [23]. Most of the materials are taken from Ref. [23][1].

2.1 Introduction

As mentioned in chapter 1, the large sheet carrier concentration at the hetero-interfaces of III-nitride HFETs typically produces a normally-on characteristic among these devices. Hence, the realization of normally-off III-nitride HFETs, which are necessary for efficient power management, single polarity power supply circuits, and safer switching in power

[1] - In [23], the basic formulation of variational method for ternary AlGaN/GaN HFETs was performed by Farzin Manouchehri, Dr. Pouya Valizadeh was the supervisor. The rest of work including applying the variational method to quaternary HFETs and analyzing the characteristics of these transistors based on the presented model were contributions of Hassan Rahbardar Mojaver.

switching applications, has been proven to be difficult. In addition to the power switching applications, based on the observations made in a few other compound semiconductor technologies on the importance of normally-off devices in improving the noise figure [24], normally-off III-nitride HFETs have also generated interest for RF applications.

Several different approaches have been proposed to realize normally-off GaN-channel HFETs [25]-[33]. One of the more promising methods is based on employing a quaternary $Al_xIn_yGa_{1-x-y}N$ barrier-layer [29]-[31], [33], using which normally-off characteristic with a threshold voltage of 0.56 V has been reported [33]. Depending on the Al and In mole-fractions (x and y) of this barrier-layer, pseudomorphic growth of the AlInGaN/GaN hetero-junction is capable of developing both tensile and compressive strain at the hetero-interface. In addition, the discontinuity of the spontaneous polarization at the hetero-interface can be controlled by these mole-fractions. Since the concentration of the 2DEG formed at III-nitride hetero-junctions is predominantly defined via the piezoelectric and the spontaneous polarizations, changing the group-III metal mole-fractions in the barrier can be used as an effective tool in engineering the threshold voltage of HFETs realized on these hetero-junctions.

Thus far, only a few investigations that include theoretical study of the 2DEG characteristics of AlInGaN/GaN hetero-junctions have been presented [22], [30]. However, determination of fermi and subband energy levels at the quaternary hetero-interface quantum well which is essential to calculation of 2DEG concentration has not been discussed in the aforementioned studies. Moreover, providing a reliable evaluation basis for the 2DEG characteristics as functions of physical and compositional properties of the quaternary hetero-junctions has been so far overlooked. This chapter aims to fulfill the

need for a more accurate theoretical evaluation of the 2DEG characteristics of AlInGaN/GaN hetero-junctions. This includes explaining the trends between the threshold voltage and physical/compositional properties of the barrier.

2.2 Calculation of physical parameters of gated metal-face wurtzite AlInGaN/GaN hetero-interface based on previous theoretical and experimental studies

In this work, the variational model formulated in [34] for AlGaN/GaN hetero-junctions, with appropriate modification of material parameters, has been used in studying AlInGaN/GaN hetero-structures[1].

Hetero-structures used in this study were composed of a thin quaternary AlInGaN barrier layer grown pseudomorphically on top of a thick GaN channel/buffer layer, where Ni established a Schottky contact to AlInGaN. In presenting the theoretical model for evaluation of 2DEG characteristics of these quaternary hetero-structures, appropriate values of polarization induced charges at the hetero-interface, conduction-band discontinuity, and Schottky barrier height had to be calculated. The details of these calculations are presented in this section.

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[1] - The variational method has been adopted in [34] to calculate the 2DEG characteristics of ternary AlGaN/GaN heterojunctions. In this model, the trial functions used for the first and second subbands are

$\psi_0(z) = \frac{1}{\sqrt{A}}[u(z)(z+\alpha)e^{-\frac{bz}{2}} + u(-z)\alpha e^{k_b z}]$

$\psi_1(z) = \frac{1}{\sqrt{B}}\left[u(z)(z+\alpha')(1-Cz)e^{-\frac{bz}{2}} + u(-z)\alpha' e^{k_b' z}\right]$,

where, z is the direction normal to the hetero-interface, b is the variational parameter, u(z) is the step function, A and B are normalization factors, C is a constant calculated by orthogonality of ψ_0 and ψ_1 and their derivatives, k_b and k_b' are wave numbers associated with the first and second subband energy levels in the barrier. In order to calculate the proper value of variational parameter (i.e., b), the total energy of the system per electron is calculated and minimized. As a result, the wavefunctions for the first two subbands are calculated.

Considering the nonlinear variations of piezoelectric polarization of Wurtzite III-nitride semiconductors with respect to metal mole-fractions, Vegard's law can be employed in evaluating the piezoelectric polarization of a polar $Al_xIn_yGa_{1-x-y}N$/GaN epilayer [35],

$$P_{PZ}\left(Al_xIn_yGa_{(1-x-y)}N\right) = xP_{PZ}(AlN) + yP_{PZ}(InN) + (1-x-y)P_{PZ}(GaN) \quad (2.1)$$

where, x and y are Al and In mole-fractions, and P_{PZ} for binaries are nonlinear functions of basal strain (μ) between $Al_xIn_yGa_{1-x-y}N$ and GaN layers.

In order to calculate the spontaneous polarization of the quaternary AlInGaN barrier-layer, Vegard's law with the incorporation of the associated nonlinearities was adopted according to [35]. The spontaneous polarization can be therefore calculated as,

$$P_{SP}\left(Al_xIn_yGa_{(1-x-y)}N\right) = xP_{SP}(AlN) + yP_{SP}(InN) + (1-x-y)P_{SP}(GaN) + b_{SP}^{AlGaN}x(1-x-y) + b_{SP}^{InGaN}y(1-x-y) + b_{SP}^{AlInN}xy \quad (2.2)$$

where, b_{SP}^{AlGaN}, b_{SP}^{InGaN}, and b_{SP}^{AlInN} are the bowing parameters of ternaries AlGaN, InGaN, and AlInN, respectively. The values of the parameters used in calculating the piezoelectric and spontaneous polarization are presented in Table 2.1.

Table 2.1 Parameters used for the calculation of piezoelectric and spontaneous polarization in AlInGaN epilayer [35].

Parameter	Value (C/m^2)
$P_{PZ}(AlN)$	-1.808×μ - 7.888×μ^2 for μ>0 -1.808×μ + 5.624×μ^2 for μ<0
$P_{PZ}(InN)$	-1.373×μ + 7.559×μ^2
$P_{PZ}(GaN)$	-0.918×μ + 9.541×μ^2
$P_{SP}(AlN)$	-0.0898
$P_{SP}(InN)$	-0.0413
$P_{SP}(GaN)$	-0.0339
b_{SP}^{AlGaN}	0.0191
b_{SP}^{InGaN}	0.0378
b_{SP}^{AlInN}	0.0709

The total polarization vector of a metal-face wurtzite III-nitride AlInGaN/GaN hetero-junction not disturbed by any external force is calculated by the summation of spontaneous and piezoelectric polarizations. Additionally, the polarization-induced charge density is the result of the divergence of the polarization along the growth direction. Therefore, the two dimensional charge density at the metal-face hetero-interface is equal to,

$$\sigma = \Delta P_{SP} + \Delta P_{PE} = [P_{SP}(AlInGaN) - P_{SP}(GaN)] + [P_{PZ}(AlInGaN) - P_{PZ}(GaN)] \quad (2.3)$$

where ΔP_{SP} and ΔP_{PZ} are the difference in spontaneous and piezoelectric polarizations between the barrier and buffer/channel layer. In order to evaluate the predictive power of the present model, Table 2.2 presents a comparison between the results obtained through (2.1) - (2.3) and the limited experimental data reported in literature.

Table 2.2 Polarization-induced sheet charge density (σ) at $Al_{0.54}In_{0.12}Ga_{0.34}N$/GaN hetero-interface calculated based on the model expressed by (2.1) - (2.3) and the sparsely available experimental data. The experimental data is provided in [36].

σ ($\mu C/cm^2$)	Method
2.14	Model expressed by (2.1)-(2.3)
2.099±0.054	Hall measurement
1.978±0.036	I_D-V_G measurement
1.968±0.133	C-V measurement

Figure 2.1 presents the bandgap versus lattice constant of $Al_xIn_yGa_{1-x-y}N$ for all possible values of *x* and *y* with indication of ΔP_{SP} equi-contours (a), ΔP_{PZ} equi-contours (b), and sheet charge density equi-contours (c) at $Al_xIn_yGa_{1-x-y}N$/GaN hetero-interface with corresponding values of *x* and *y*. The bandgap of the quaternary AlInGaN was estimated

using Vegard's law by employing the ternary alloy bowing parameters according to the following equation [37]:

$$E_G(AlInGaN) = (1-x-y)E_G(GaN) + xE_G(AlN) + yE_G(InN) - b_{EG}^{AlGaN}x(1-x) - b_{EG}^{InGaN}y(1-y) - (b_{EG}^{AlInN} - b_{EG}^{AlGaN} - b_{EG}^{InGaN})xy. \quad (2.4)$$

The values used for the bandgap of binary end-points and ternary bowing parameters are presented in Table 2.3. It should be noted that the bandgap-related bowing parameters of III-nitrides are still under investigation [37]-[39]. Regarding Fig. 2.1(a), the contours show approximately similar value of spontaneous polarization for the layers with identical value of Al mole-fraction. This is because the high spontaneous polarization of AlN in comparison with GaN and InN makes the spontaneous polarization of AlInGaN to depend mainly on the Al mole-fraction. However, according to Fig. 2.1(b), for moderate values of *x* and *y* contours of piezoelectric polarization are defined almost vertically, which confirms the dependence of piezoelectric polarization on basal strain and consequently lattice constant of the AlInGaN layer.

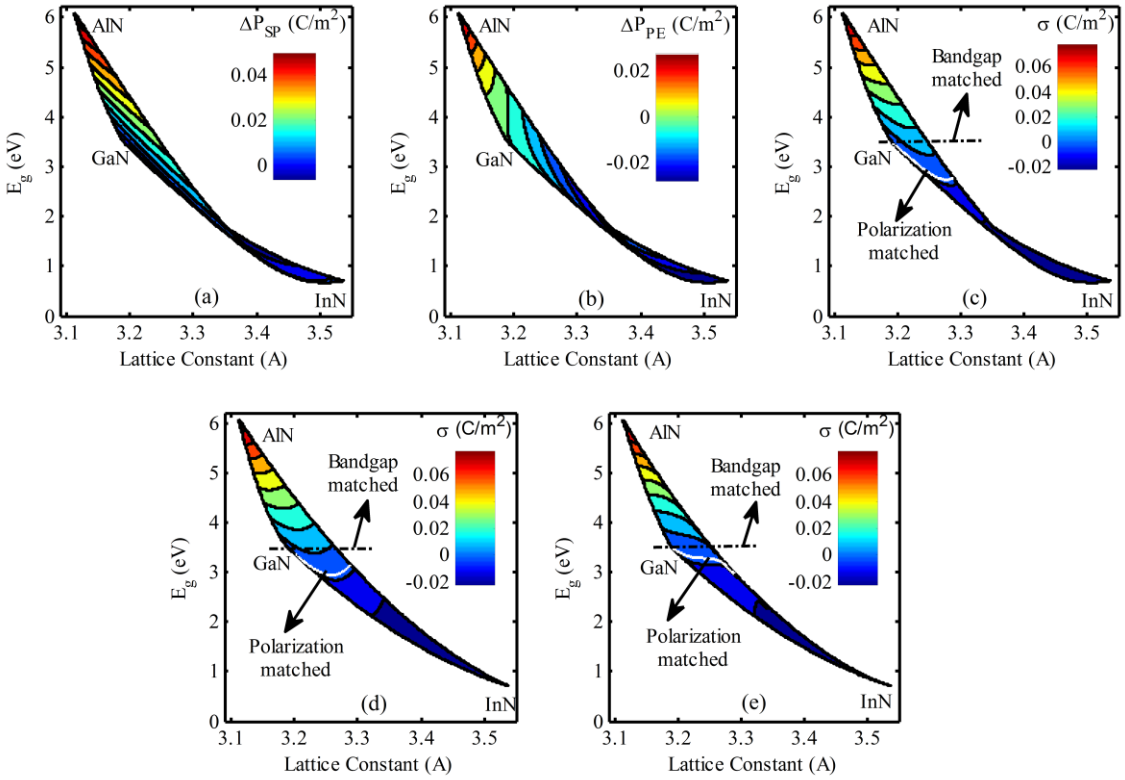


Figure 2.1 Bandgap vs. lattice constant for $Al_xIn_yGa_{1-x-y}N$ quaternary barrier-layer with indication of ΔP_{SP} equi-contours (a), ΔP_{PZ} equi-contours (b), and sheet charge density equi-contours (c) at $Al_xIn_yGa_{1-x-y}N$/GaN hetero-interface for the corresponding values of x and y. (d) and (e) represent plots identical to (c) if the bandgap is calculated using the bowing parameters presented in [38] and [39], respectively.

Table 2.3 Bandgap of binary III-Nitrides and ternary bowing parameters of bandgap [37].

Parameter	Value (eV)
$E_G(GaN)$	3.45
$E_G(AlN)$	6.21
$E_G(InN)$	0.68
b_{EG}^{AlGaN}	0.9
b_{EG}^{InGaN}	1.72
b_{EG}^{AlInN}	$\frac{6.43}{1+1.21x^2}$

Figure 2.1 (c) illustrates the total polarization-induced sheet charge density at the hetero-interface. As previously mentioned, the quaternary barrier-layer provides us with the capability of engineering both the bandgap and the total polarization effect at the hetero-interface. In this figure, the corresponding contour for which the sheet charge density is equal to zero is indicated. The corresponding border at which the bandgap of the barrier and buffer/channel layer are matched is also highlighted. Based on the results depicted in Fig. 2.1 (c), an interesting observation is that, contrary to the previously claimed possibility of offering polarization-matched quaternary hetero-junctions while retaining the large bandgap of the barrier-layer and the resulting proper carrier confinement [21], [33], [40], this structure is not capable of implementing this twofold characteristic simultaneously. In other words, as evident from Fig. 2.1 (c), for a polarization-matched barrier-layer, the buffer/channel layer exhibits a larger bandgap, which rules out the possibility of developing a quantum-well at the hetero-interface. Therefore, no carrier confinement exists in this condition. Although exact matching of polarization is not possible, quaternary barriers can still help design devices with low interface polarization charge. Figures 2.1 (d) and (e) show the total polarization-induced sheet charge density if the bandgap of the barrier is calculated using the bowing parameters presented in [38] and [39], respectively. These

figures confirm that independent of the choice of reference for the bowing parameters a similar observation on the inability of polarization-matched barriers to produce a positive conduction-band discontinuity is made.

For the calculation of conduction-band discontinuity (ΔE_C), it should be considered that thus far there has been little work dedicated to evaluation of (ΔE_C) of III-nitride quaternary AlInGaN/GaN hetero-junctions. According to [41], ΔE_C is evaluated as the difference between the discontinuity of the bandgap and that of the valence band (i.e. ΔE_V). The ratios of $\Delta E_C/\Delta E_V$ for AlN/GaN, GaN/InN, and AlN/InN are reported as 70:30, 60:40, and 70:30, respectively [42].

A framework according to Vegard's law was adopted by Satpathy *et al.* for calculation of ΔE_V of ternary AlGaN/GaN hetero-junctions [43]. However, lack of existing knowledge about bowing parameters associated with ΔE_V of quaternary AlInGaN/GaN hetero-junctions renders the same approach incapable of accurately evaluating the corresponding ΔE_C values. Taking into account that throughout our current study In mole-fraction has to be smaller than that of Al (i.e. in order to keep the bandgap of AlInGaN barrier larger than the bandgap of GaN), in this case the $\Delta E_C/\Delta E_V$ ratio can be assumed as 70:30, similar to the value which is usually used for AlGaN/GaN hetero-structures [35], [44].

In this work, the Schottky barrier height was calculated assuming a Ni metal gate in contact with AlInGaN. Considering the Schottky barrier lowering, the barrier height is calculated according to,

$$q\phi_B(V_{GS}) = q\phi_{m(Ni)} - q\chi_{AlInGaN} - \sqrt{\frac{q^3 E(V_{GS})}{4\pi\epsilon_{AlInGaN}}} \tag{2.5}$$

where q is the elementary charge, $q\phi_{m(\mathrm{Ni})}$ is the work-function of Ni, $q\chi_{\mathrm{AlInGaN}}$ is the electron-affinity of AlInGaN, $\epsilon_{AlInGaN}$ is the low-frequency permittivity of AlInGaN, V_{GS} is

the gate-source voltage, and $E(V_{GS})$ is the electric field across the barrier-layer. The electron-affinity of the quaternary AlInGaN can be estimated applying Vegard's law [35]. The expected uncertainty from this operation is intensified especially in case of high In mole fractions. This is since InN's electron-affinity can be determined with less precision compared to that of AlN and GaN [45]. As previously noticed, In mole fraction of AlInGaN barriers in the current study has to be small to guarantee the larger bandgap of AlInGaN barrier with respect to GaN. Hence, applying Vegard's law for calculation of electron-affinity in quaternary AlInGaN is deemed acceptable.

Since in the polar III-nitride system the polarization effect plays a dominant role in inducing the electric field across the barrier-layer, it is reasonable to assume a triangular potential barrier formed across this layer. As a result, the electric field across the barrier layer $E(V_{GS})$ based on [44],[9], is given by,

$$E(V_{GS}) = \frac{(q\phi_B - qV_{GS}) + E_F - \Delta E_C}{q d_{AlInGaN}} \tag{2.6}$$

where E_F is the fermi level and d_{AlInGaN} is the thickness of the barrier-layer.

2.3 Evaluation of 2DEG characteristics using variational method

The 2DEG characteristics including 2DEG concentration (n_s), first and second subband energy levels (E_0 and E_1), and the position of fermi energy level were evaluated according to the procedure presented in Fig. 2.2. The calculation procedure starts by assuming an initial position for the fermi level (i.e., the lower edge of the conduction-band of GaN at

the hetero-interface). Using (2.5) and (2.6) ϕ_B and E, which are mutually dependent, are calculated using an iterative approach. 2DEG concentration can be calculated in two ways. Firstly, from the Gauss' law at hetero-interface,

$$n_s = \frac{\sigma - \epsilon_{AlInGaN} E}{q}. \tag{2.7}$$

Secondly, in terms of the density of states function of the first and second subbands,

$$n_s = D_S \frac{kT}{q} \left\{ ln\left[1 + exp\left(\frac{E_f - E_0}{kT}\right)\right] + ln\left[1 + exp\left(\frac{E_f - E_1}{kT}\right)\right]\right\} \tag{2.8}$$

in which, D_S is two-dimensional density of states, k is the Boltzmann constant, and T is the temperature in kelvin. According to [34], E_0 and E_1 can be calculated through minimization of the total energy per electron using variational method as a function of E. In an iterative approach E_f is gradually increased until the values obtained from (2.7) and (2.8) converge with the relative error of less than 0.1%. For calculating the threshold voltage, n_s is considered as zero, and (2.7)-(2.8) are re-evaluated to find the corresponding V_{GS} which makes n_s equal to zero using the similar procedure.

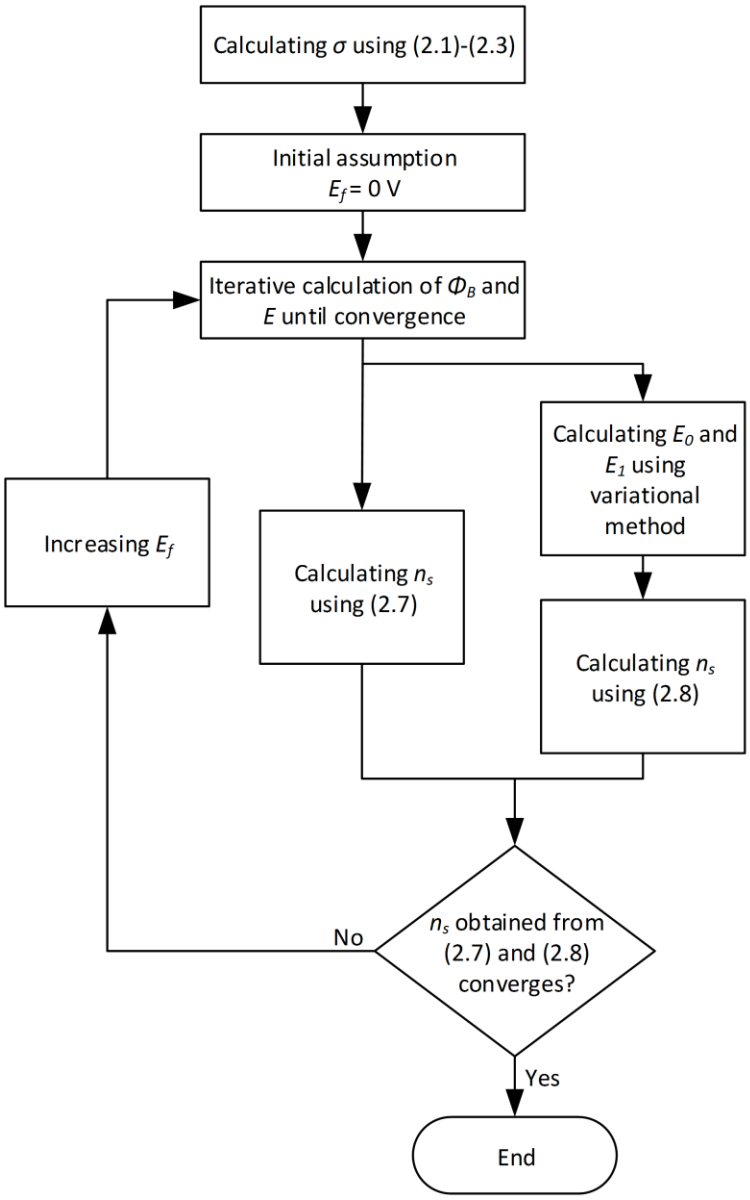


Figure 2.2 Flowchart of the procedure for evaluation of 2DEG characteristics.

2.4 Validating the accuracy of presented model versus the experimental results reported in different studies

The accuracy of the model has been validated versus the 2DEG concentrations of the experimentally analyzed quaternary polar III-nitride samples reported in different studies. Employing a Ni Schottky contact, Table 2.4 compares the calculated values of the 2DEG

characteristics with published experimental data. The acceptable overall match between measurements and calculations is a testimony to the accuracy of the model. Hence, in case of the samples for which the experimental results are not available, the current study can assist in forecasting the 2DEG characteristics.

Table 2.4 Simulation results of the physics-based model for the 2DEG characteristics of AlInGaN/GaN hetero-junctions previously reported in the literature.

Metal mole-fraction					Current study simulation			Experimental results			
Al	In	Ga	$d_{AlInGaN}$ (nm)	ϕ_B (V)	n_s (cm^{-2})	σ (C/m^2)	V_{th} (V)	n_s (cm^{-2})	V_{th} (V)	Error for n_s (%)	Ref.
0.74	0.16	0.1	12.5	2.21	2.02×10^{13}	0.0324	-4.9	1.81×10^{13}	-5.2	+11.60	[21],[46]
0.7	0.15	0.15	11.8	2.14	1.53×10^{13}	0.037	-3.54	1.61×10^{13}	-4.5	-4.97	[21],[46]
0.66	0.14	0.2	10.3	2.07	1.32×10^{13}	0.034	-2.71	1.52×10^{13}	-3.8	-13.16	[21],[46]
0.48	0.17	0.35	8	1.68	1.58×10^{12}	0.018	-0.23	1.80×10^{12} [a]	0.56	----	[33]
0.11	0.02	0.87	8	1.09	----[b]	0.0047	0.63	8.00×10^{11}	0.2	----	[33]
0.16	0.02	0.82	20	1.19	2.19×10^{12}	0.0075	-9.17	1.80×10^{12}	----[c]	+21.67	[47]
0.34	0.03	0.63	20	1.54	8.37×10^{13}	0.0185	-3.46	1.13×10^{13}	----[c]	+25.93	[47]
0.52	0.03	0.45	20	1.90	1.70×10^{13}	0.0332	-6.99	2.29×10^{13}	----[c]	-25.76	[47]
0.72	0.14	0.14	5.6	2.19	1.15×10^{13}	0.0394	-1.38	1.13×10^{13}	----[c]	+1.77	[48]
0.73	0.11	0.16	5.3	2.24	1.40×10^{13}	0.0439	-1.63	1.36×10^{13}	----[c]	+2.94	[48]
0.73	0.11	0.16	15	2.24	2.14×10^{13}	0.0439	-6.33	2.14×10^{13}	----[c]	0.00	[48]
0.75	0.07	0.18	4.4	2.32	1.72×10^{13}	0.0512	-1.76	1.42×10^{13}	----[c]	+21.13	[48]
0.75	0.07	0.18	4.8	2.32	1.80×10^{13}	0.0512	-1.98	1.96×10^{13}	----[c]	-8.16	[48]
0.75	0.07	0.18	6.8	2.32	2.10×10^{13}	0.0512	-3.11	2.37×10^{13}	----[c]	-11.39	[48]

All of the devices are assumed to use a Ni gate.

[a] The reported value is corresponding to the ungated region, hence no comparison is made to the theoretically evaluated value.

[b] This is an enhancement-mode device, thus, at $V_{GS} = 0$ V, 2DEG is already depleted and there is no quantum well. As a result, variational method cannot be used for evaluation of n_s. n_s would be almost equal to the background doping.

[c] No value has been reported.

2.5 Analyzing the effect of physical and compositional properties of the hetero-junction on different characteristics of the AlInGaN/GaN HFETs

Figure 2.3 illustrates the calculated conduction-band edge diagrams of metal-face polar $Al_{0.3}Ga_{0.7}N$/GaN and $Al_{0.3}In_{0.1}Ga_{0.6}N$/GaN hetero-junctions of 20 nm thick barrier. As can be observed from this figure, for the latter set of mole-fractions (i.e., $x = 0.3$ and $y = 0.1$) a pronounced reduction of the polarization effect prevents the quantum-well at the hetero-interface from attracting enough carriers to form the 2DEG. For a constant Al mole-fraction, as In mole-fraction increases, the tensile strain in the barrier-layer decreases and eventually turns into a compressive strain (hence, changing the direction of the piezoelectric polarization in the over-layer), while spontaneous polarization remains nearly constant. This is since the Al mole-fraction has not changed. As a result, total polarization is reduced. In an AlInGaN/GaN HFET reducing the polarization will lead to lower 2DEG carrier density and increase in the on-resistance of the device. Accordingly, it causes the threshold voltage to shift in the positive direction thereby producing an enhancement-mode device. Figure 2.4 presents the variation of threshold voltage of gated AlInGaN/GaN hetero-junctions versus the In mole-fraction for three different values of Al mole-fraction. Replacing Ga atoms with In (i.e., increasing In mole-fraction while Al mole-fraction remains constant) or Al atoms with In (i.e., increasing In mole-fraction while decreasing Al mole-fraction) can both increase the threshold voltage.

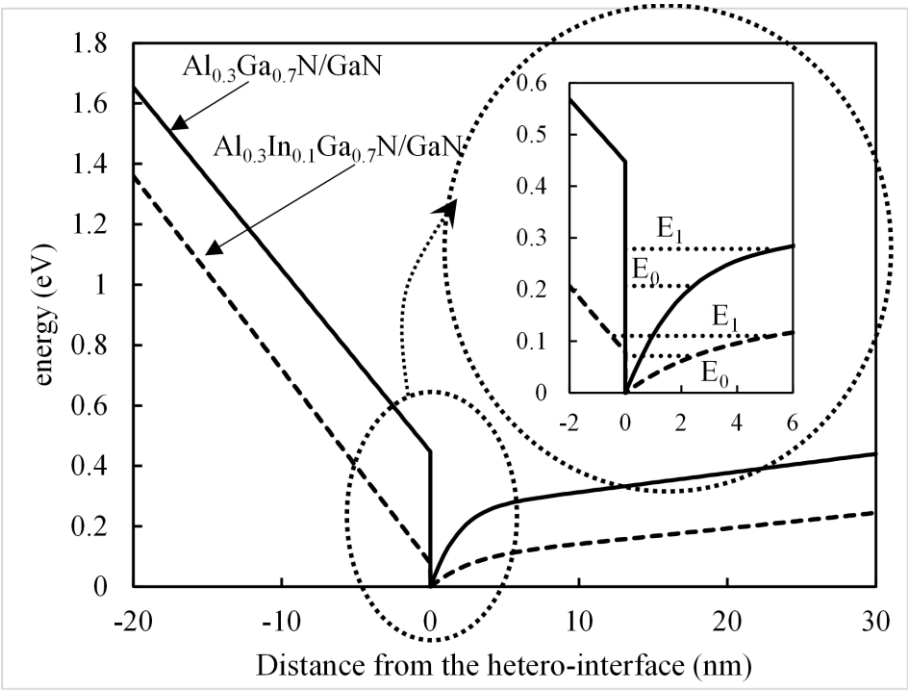


Figure 2.3 Conduction-band edge diagrams of $Al_{0.3}Ga_{0.7}N/GaN$ (black line) and $Al_{0.3}In_{0.1}Ga_{0.6}N/GaN$ (dashed line) hetero-junctions. The inset shows the first and second subband energy levels in the quantum well for each hetero-interface. The barrier thickness is 20 nm.

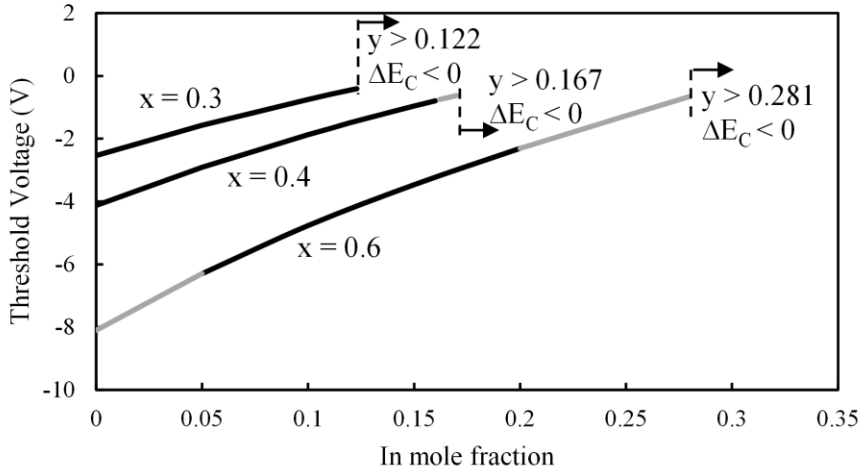


Figure 2.4 Simulation results presenting the variation trend of threshold voltage of gated AlInGaN/GaN hetero-junctions (for Al mole-fractions of 0.3, 0.4, and 0.6) with the same barrier thickness of 20 nm versus In mole-fraction. The gray portions of each characteristic highlight the In mole-fractions which render the 20 nm thickness of the barrier in excess of the strain-defined critical thickness. The limit of In mole fraction beyond which ΔE_C becomes negative is also indicated on each curve.

Variations of 2DEG concentration and threshold voltage of AlInGaN/GaN HFETs as functions of In mole-fraction and barrier thickness are illustrated in Fig. 2.5. Considering the variation of both the spontaneous and the piezoelectric polarizations, total polarization effect decreases with increasing In mole-fraction. This in turn reduces the density of the polarization-induced charges at the hetero-interface. The depleting effect of the Schottky barrier is also observed to result in lower electron concentration, and the positive shift in threshold voltage, when the barrier becomes thinner. It is worth mentioning that the detrimental effect of crack formation in the barrier-layer at thicknesses beyond the critical thickness is not included in the theoretical evaluation.

According to these observations, in order to realize an enhancement-mode HFET, higher In mole-fraction and thinner barrier should be employed simultaneously. Figure 2.6(a) through depicting contours of threshold voltage for different metal mole-fractions highlights the applicable compositional window for the realization of enhancement-mode characteristic when the barrier thickness is 10 nm. Figure 2.6 (b) illustrates the contours of V_{th} = 0 V for different values of barrier thickness. Based on this figure, for the devices employing thinner barriers, threshold voltage of zero can be realized at lower values of In mole-fraction. Similar threshold voltages for the devices with almost equal ratio of Al and In mole-fractions can be interpreted from both panels of Fig. 2.6.

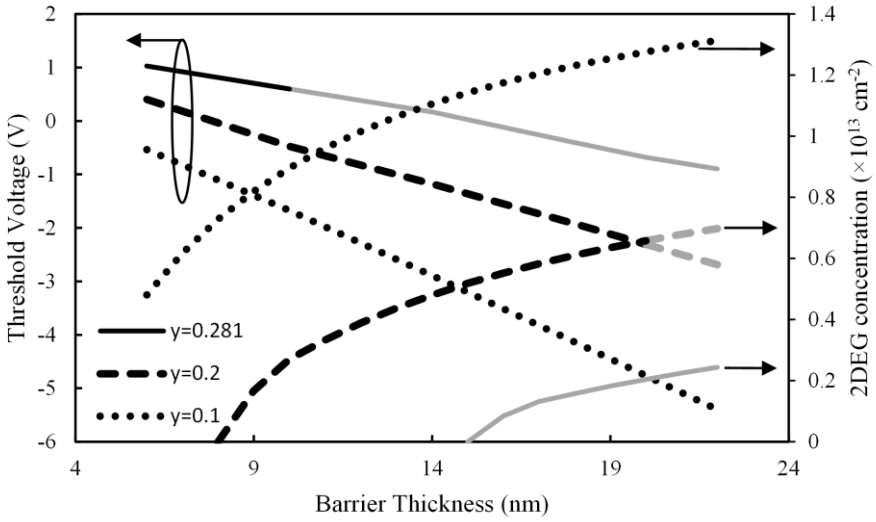


Figure 2.5 Simulation results illustrating the 2DEG concentration and threshold voltage of AlInGaN/GaN HFETs versus barrier thickness for Al mole-fraction of 0.6 and three different In mole-fractions of 0.1, 0.2, and 0.281. The 2DEG concentrations are presented for V_{GS} = 0 V. In $Al_{0.6}In_{0.281}Ga_{0.119}N$/GaN and $Al_{0.6}In_{0.2}Ga_{0.2}N$/GaN HFET when the barrier is thinner than 15 and 8 nm, respectively, the 2DEG is completely depleted. The gray portions of each characteristic highlight the barrier thicknesses which are in excess of the strain-defined critical thickness. For Al mole fraction of 0.6, In mole fraction of 0.281 is the upper limit beyond which ΔE_C becomes negative.

Figure 2.7 presents variations of the subband energy levels and the fermi level as functions of *y*, for different values of *x*. According to the simulation results, increasing *y* exhibits the same effect as decreasing *x*, which causes the positions of the two subband energy levels to converge while the fermi energy levels decrease. A possible explanation for these observations can be found in reduction of the polarization effect caused by In incorporation, which results in weaker carrier confinement. In this condition, the hetero-interface quantum well gets wider and shallower. Although 2DEG subband levels get closer, as the relative position of fermi level with respect to E_0 and E_1 drops, the probability of occupation of free states in these subbands decreases. As a result, 2DEG can be depleted more easily yielding an enhancement-mode device.

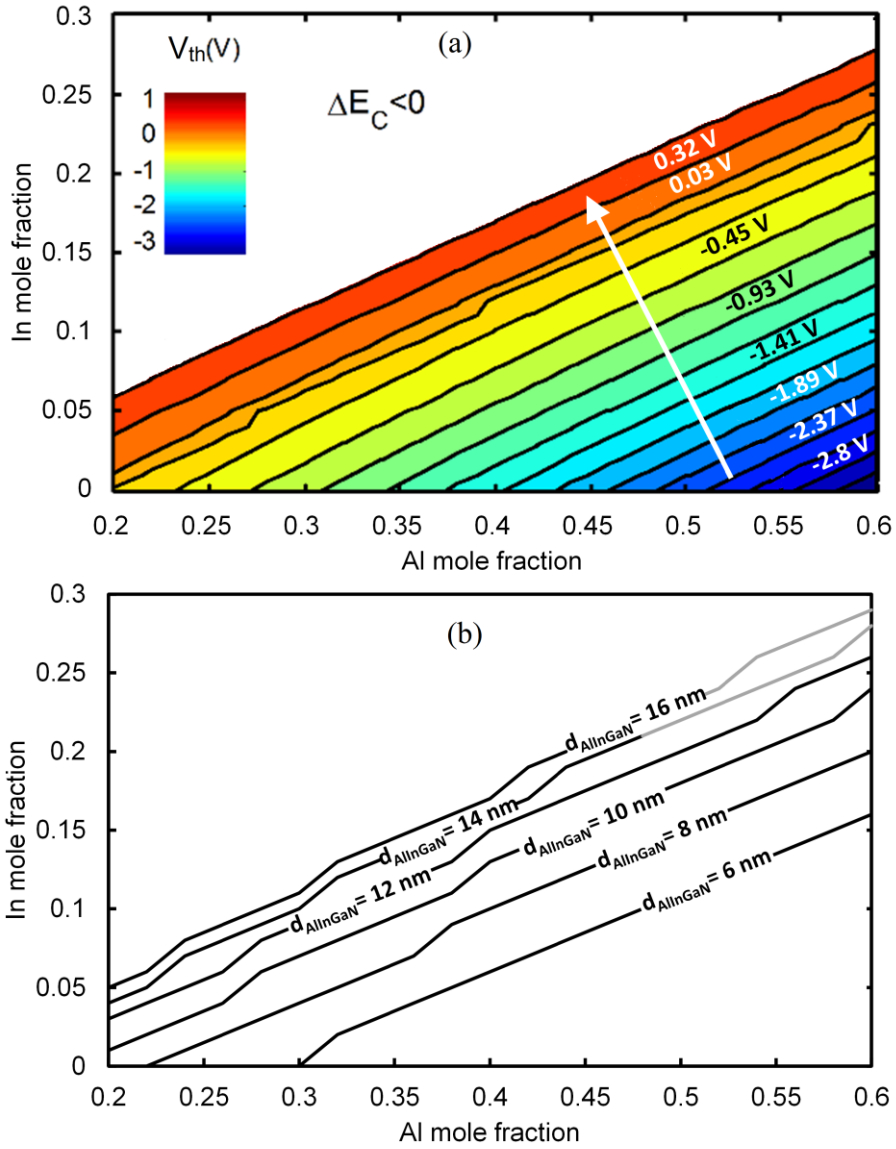


Figure 2.6 (a) Simulation results presenting contours of threshold voltage of gated AlInGaN/GaN HFETs for different values of Al and In mole fractions. The barrier thickness is 10 nm. (b) Contours of V_{th} = 0 V for different values of barrier thickness. In (b), the gray portions of each characteristic highlight the barrier thicknesses which are in excess of the strain-defined critical thickness at the corresponding metal mole-fractions.

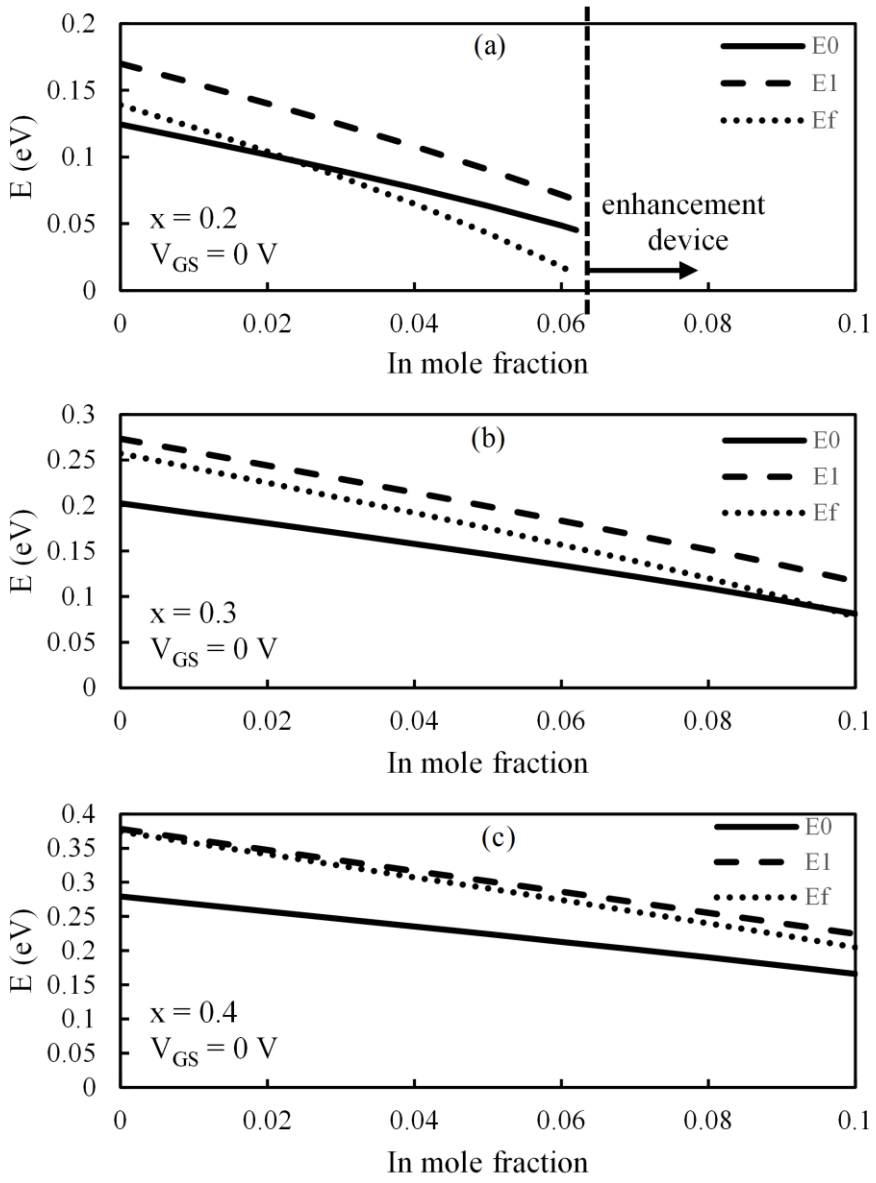


Figure 2.7 Illustration of the first and second subband energy levels (i.e., E_0 and E_1) and fermi energy level (i.e., E_F) as functions of In mole-fraction, for different values of Al mole-fractions when V_{GS} = 0 V. The barrier thickness is 20 nm. The reference for all energy levels is the energy level of conduction-band edge at hetero-interface.

Initial inspection of Fig. 2.7 also reveals that increase in y results in the fermi energy level lying further from the second subband energy level. Therefore, it might be deduced that consideration of the second subband energy level is in vain. However, it should be noted that the results presented in this figure are based on the hetero-junctions with V_{GS} = 0 V whereas the hetero-junctions with higher In mole-fractions normally operate at higher V_{GS}

values. For clarifying the effect of V_{GS}, Fig. 2.8 provides variations of the subband energy levels and the fermi level as functions of V_{GS} for an $Al_{0.4}In_{0.05}Ga_{0.55}N$/GaN HFET. According to the simulation results, increasing the gate-source voltage imposes an effect opposite to that of higher In mole-fraction on the position of subband energy levels versus the fermi level. As a result, as in ternary AlGaN/GaN hetero-junctions for quaternary hetero-junctions it would not be reasonable to ignore the presence of the second subband energy level.

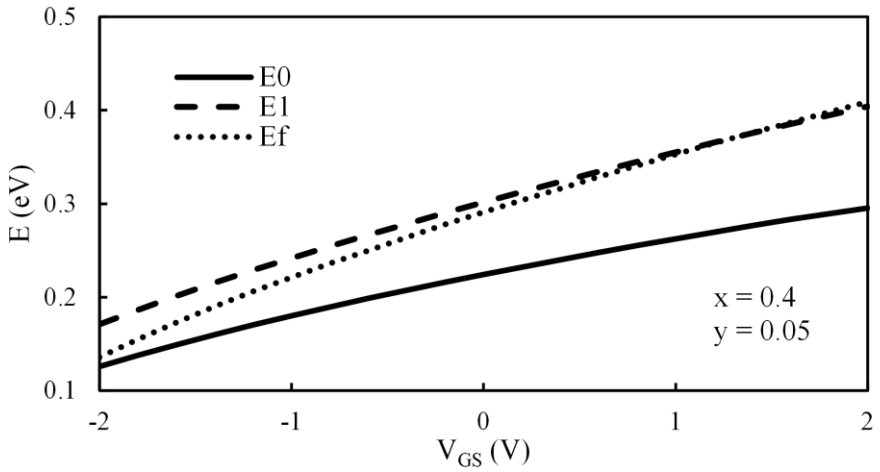


Figure 2.8 Illustration of the first and second subband energy levels (i.e., E_0 and E_1) and fermi energy level (i.e., E_F) as functions of V_{GS} for $Al_{0.4}In_{0.05}Ga_{0.55}N$/GaN HFET. The reference for all energy levels is the energy level of conduction-band edge at hetero-interface. The barrier thickness is 20 nm.

Employing a commercial Poisson-Schrödinger solver validity of the variational method is assessed when the conduction-band discontinuity is relatively small. In the assessment employing the commercial package *Nextnano* [49], the wavefunctions for the first and second subbands (ψ_0 and ψ_1) considering different metal mole-fraction have been compared to the results obtained from the variational calculations.

Figure 2.9 compares the wavefunctions calculated using *Nextnano* and the developed variational code for the first and second subbands of $Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ and $Al_{0.82}In_{0.18}N/GaN$ HFETs with relatively small and large ΔE_C values (i.e. 0.19 eV and 0.87 eV, respectively). The wavefunctions calculated using the two methods for the first subbands have been found to be quite similar. The correlation coefficient between the functions calculated for the $Al_{0.82}In_{0.18}N/GaN$ HFET is 0.9990, while for $Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ this value is 0.9968. There is a small mismatch among the wavefunctions calculated using the two methods for the second subbands. However, this mismatch does not considerably expand as ΔE_C decreases. The correlation coefficient between the calculated ψ_1's for $Al_{0.82}In_{0.18}N/GaN$, and $Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ is 0.8640, and 0.8926, respectively.

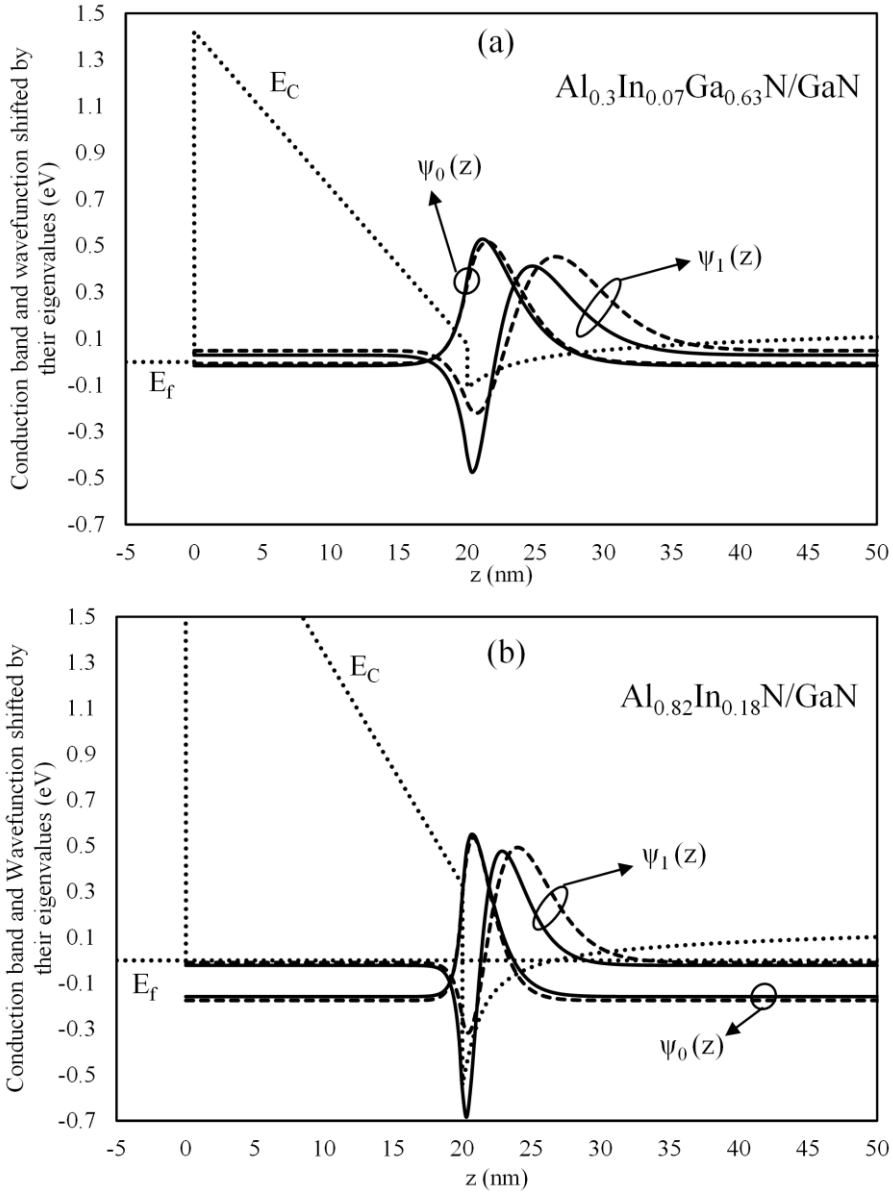


Figure 2.9 Conduction-band edge (E_C) and the wavefunctions related to the first and second subbands (ψ_0 and ψ_1) for (a) $Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ and (b) $Al_{0.82}In_{0.18}N/GaN$ HFETs at V_{GS}=0 V. Wavefunctions are normalized to 1 $nm^{-1/2}$ and shifted by their eigenvalues. Wavefunctions presented in full line and dashed line are calculated using variational method and Poisson-Schrödinger self-consistent solver, respectively.

2.6 Conclusion

The 2DEG characteristics of AlInGaN/GaN hetero-junctions are theoretically modeled using the variational method. It is confirmed that the threshold voltage of a quaternary GaN-based hetero-junction can be increased to values above zero by engineering both the spontaneous and the piezoelectric polarization. Furthermore, this study reveals that in obtaining this end-goal, reducing the polarization through attempting a polarization-matched hetero-structure is not capable of offering the chance of channel formation on the GaN side of the hetero-junction. Hence, a coordinated use of relatively thin barrier (i.e., to enhance Schottky depletion) and strain engineering via incorporation of In in the barrier is needed to warrant a positive threshold voltage. The calculated 2DEG concentrations based on the present theoretical evaluation agree with the experimental values reported in the literature. Results show that the first and second subbands become closer and the position of fermi level reduces as In mole-fraction increases or Al mole-fraction decreases.

Chapter 3

Use of a bilayer lattice-match AlInGaN barrier for improving the channel carrier confinement of enhancement-mode AlInGaN/GaN hetero-structure field-effect transistors

The contributions of this chapter have been already published [50]. Most of the materials are taken from Ref. [50][1].

3.1 Introduction

Although several studies have so far reported on the threshold-voltage engineering in quaternary AlInGaN/GaN HFETs [22], [23], [29], [30], [33], quantitative assessment of

[1] - In [50], *Nextnano* modeling is performed by collaboration of Hassan Rahbardar Mojaver and Jean-Lou Gosselin, Dr. Pouya Valizadeh was the supervisor, and the rest of work including proposing the new bilayer lattice-match barrier and investing its effect on the performance of quaternary HFETs were contributions of Hassan Rahbardar Mojaver.

the degree of carrier confinement to the GaN channel in the so-called 2DEG has remained unnoticed. Since the realization of lattice-matching between the quaternary barrier and the GaN channel has been proven to come at the unfortunate cost of reduced conduction-band discontinuity [23], leaking of the electronic wave-function of the first and especially higher subbands to the barrier seems inevitable. Such a leakage causes an increased exposure to the scattering mechanism such as alloy and interface roughness scattering, which will induce degradation in mobility and eventually the current drive of the transistor. Since in the intended enhancement-mode HFETs the transistor is often operating under a positive gate voltage, this is a problem that is much aggravated beyond the thermal-equilibrium expectations.

As a solution to the problem of carrier confinement (and also for improving the 2DEG mobility), so far a number of investigators have looked into incorporation of a very thin AlN spacer layer between the GaN channel and the AlInGaN barrier [22], [33], [51]-[53]. However, although thin, the incorporation of the AlN spacer is expected to result in a tangible negative shift of the threshold-voltage, caused by increasing the spontaneous polarization discontinuity and induction of strain between the channel and the spacer. Consequently, while successful in improving the conduction-band discontinuity (and the carrier confinement), the addition of the AlN spacer to the hetero-structure expectedly partially negates the gains of employing a lattice-match barrier for achieving a positive value of threshold-voltage. Such a loss can be only compensated by taking advantage of the other techniques used in positive-shifting the threshold-voltage of GaN-channel HFETs, such as barrier-thinning [54],[55], which will come at a certain cost (in this specific case, being the worsening of the gate-leakage problem via the thinned barrier). In order to

avoid the complications attributed to the use of AlN spacer, this chapter looks into employing a lattice-match spacer layer of inferior spontaneous polarization to AlN for achieving the required enhancement to the conduction-band discontinuity (and as a result, carrier confinement). Using the commercial self-consistent Poisson-Schrödinger solver *Nextnano* [49], a quantitative assessment of the gains of employing the proposed epilayer versus AlInGaN/AlN/GaN for achieving a better confined 2DEG in enhancement-mode HFETs is presented.

3.2 Device structure

The layer structures for the HFETs which are investigated in this study are depicted in Fig. 3.1. As shown in this figure, the simulated pseudomorphic epitaxial layer structures were assumed to consist of a substrate, followed by a thick undoped-GaN buffer/channel layer, while a 10 nm thick barrier capped by a Ni Schottky gate forms a hetero-junction to the GaN channel. Based on the composition of the barrier layer, the studied HFETs are divided into three groups.

Group 1 comprises of lattice-match quaternary $Al_xIn_yGa_{1-x-y}N$/GaN HFETs without a spacer layer. The barrier/spacer layers of HFETs in group 2 consist of 9 nm thick lattice-match $Al_xIn_yGa_{1-x-y}N$ layer and a 1 nm thick AlN spacer. Group 3 represents the proposed lattice-match $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N/Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$/GaN HFETs, in which the barrier is divided into two separate lattice-match AlInGaN layers of different metal mole-fractions. In this latter group of HFETs, the choice of metal mole-fractions in the $Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$ spacer layer is partially made for improving the ΔE_C to the GaN channel. While the thicknesses of the barrier and spacer layer in the first two groups were chosen in

consistence with the average reported values for enhancement-mode AlInGaN/GaN HFETs (i.e. variable from 8 nm to 15 nm) [33], [51], the total thickness of the barrier/spacer in group 3 was taken equal to that of group 1 to allow similar device manifestation (e.g. gate depletion effect). However, in this case the alloyed nature of the spacer limits the thickness of this layer to a minimum of about 2 nm (i.e. about six times the lattice-constant).

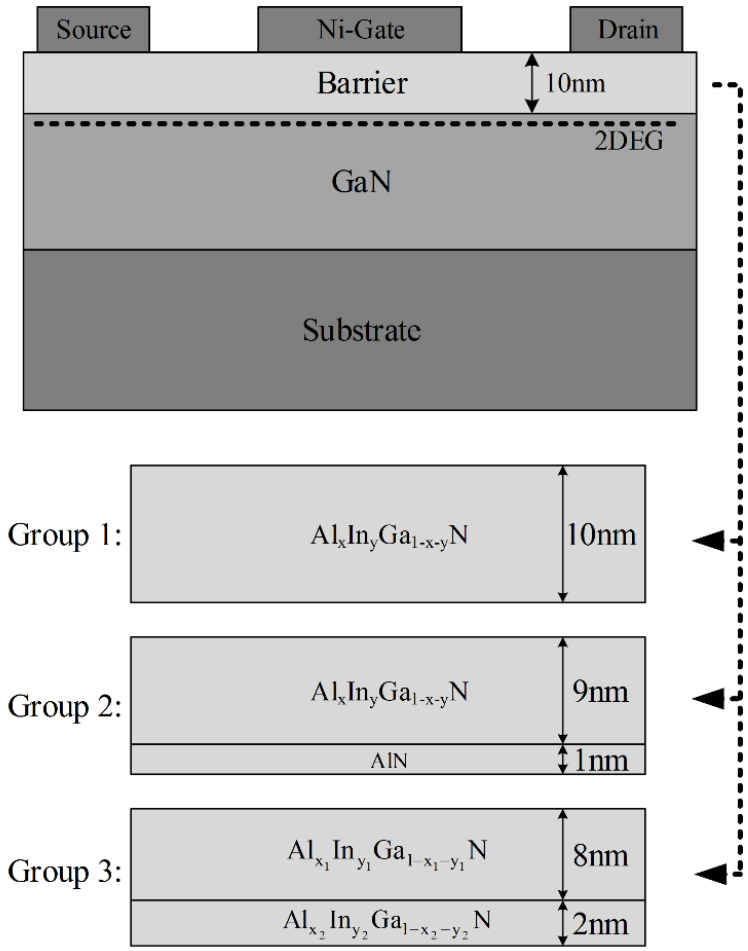


Figure 3.1 Cross-sectional view of a quaternary GaN-channel HFET. Based on the composition of the barrier-layer, the studied HFETs are divided into three groups.

3.3 Results and discussions

Figure 3.2 presents the variation of bandgap versus lattice constant for $Al_xIn_yGa_{1-x-y}N$ layers with indication of sheet charge density equi-contours at the $Al_xIn_yGa_{1-x-y}N$/GaN hetero-interface for different Al and In mole-fractions. Details of the calculations performed for metal-face c-plane wurtzite epilayers, which are presented in this figure, were thoroughly discussed in chapter 2. On this figure, shown by the black dots sitting on a straight-line indicating the lattice constant of GaN, seven different sets of metal mole-fractions for the lattice-match quaternary $Al_xIn_yGa_{1-x-y}N$ layer are highlighted. These are the mole-fractions that are used in investigating the effect of these parameters on the carrier confinement among the three aforementioned groups of transistors. According to this figure, by reducing the Al mole-fraction, in addition to the bandgap of the barrier, the polarization-induced sheet charge density at the lattice-match $Al_xIn_yGa_{1-x-y}N$/GaN hetero-interface decreases among the seven highlighted compositions from $Al_{0.82}In_{0.18}N$/GaN to $Al_{0.2}In_{0.04}Ga_{0.76}N$/GaN. The indicated reduction in the bandgap is associated with a reduction in ΔE_C. As mentioned earlier, the observed co-existence of these two trends among the HFETs of group 1 results in worsening of the carrier confinement as the threshold-voltage is pushed towards positive values. As an example, Fig. 3.3 presents the thermal-equilibrium conduction-band diagram under the gate electrode of two transistors of group 1 (i.e. two transistors with barriers of different metal mole-fractions). As shown in this figure, between $Al_{0.5}In_{0.11}Ga_{0.39}N$/GaN and $Al_{0.82}In_{0.18}N$/GaN, the former presents a smaller ΔE_C, while as expected from Fig. 3.2, a less negative threshold-voltage.

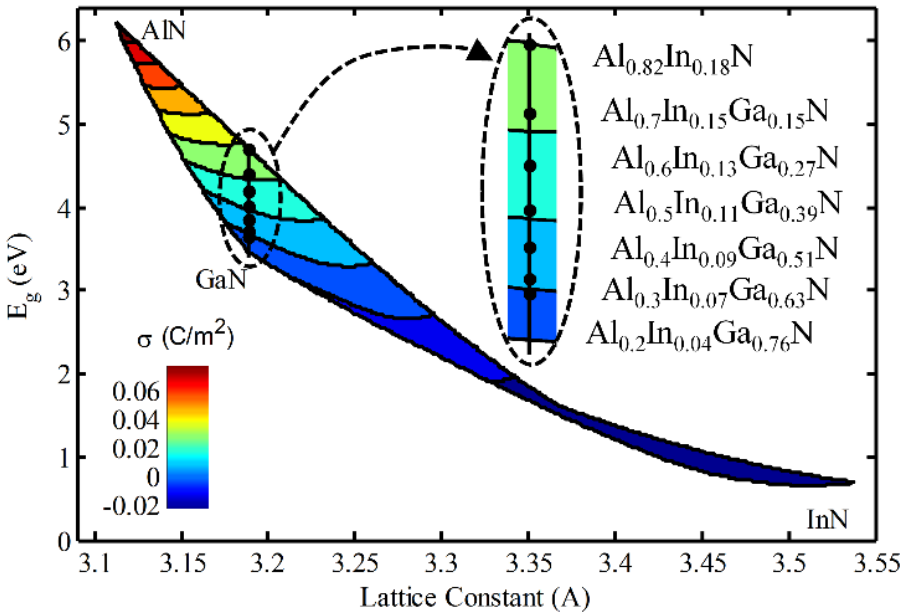


Figure 3.2 Bandgap versus lattice constant for $Al_xIn_yGa_{1-x-y}N$ barrier-layer with indication of sheet charge density (σ) equi-contours at $Al_xIn_yGa_{1-x-y}N$/GaN hetero-interface for the corresponding values of Al and In mole fractions. The black points indicate the position of lattice-match $Al_xIn_yGa_{1-x-y}N$ layers which are used in this study

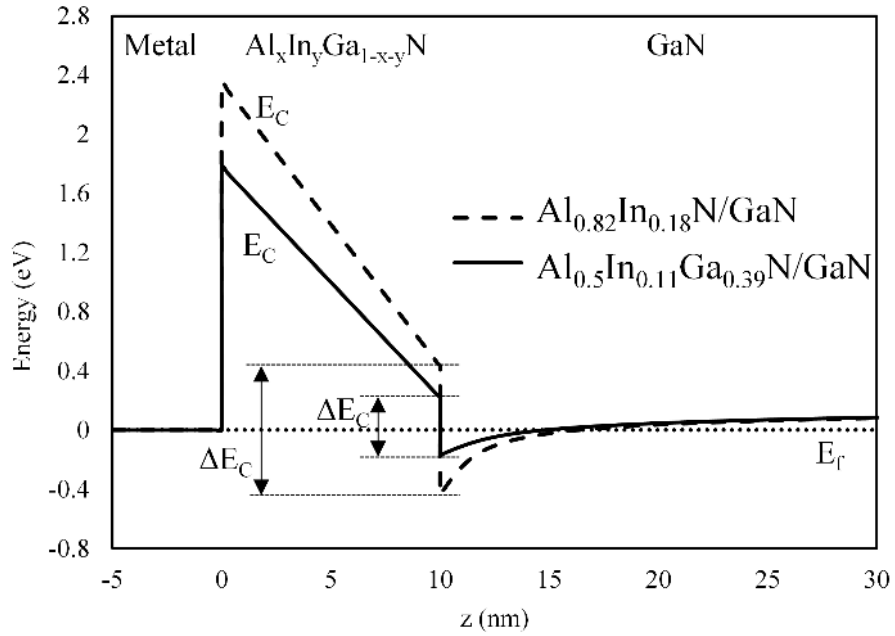


Figure 3.3 Thermal-equilibrium conduction-band (E_C) diagrams of Ni-gated $Al_{0.5}In_{0.11}Ga_{0.39}N$/GaN (full line) and $Al_{0.82}In_{0.18}N$/GaN (dashed line) HFETs. E_f indicates the fermi-level and z is the axis normal to the hetero-interface.

To present a quantitative assessment of carrier confinement to the GaN channel, using the commercial self-consistent solver *Nextnano*, electron concentration (n_s) as a function of the distance from the gate-metal/$Al_xIn_yGa_{1-x-y}N$ Schottky contact (z) was calculated among all three of the aforementioned groups of HFETs. In these calculations, n_s was evaluated using the computed wavefunctions of the first five subbands. Considering many subbands is especially consequential when the carrier confinement is poor. Figure 3.4 compares the form of the first five computed wavefunctions for the two examples of $Al_{0.4}In_{0.09}Ga_{0.51}N$/GaN, and $Al_{0.82}In_{0.18}N$/GaN. Better confinement of the wavefunctions in case of the latter HFET structure can be observed in this figure. According to these calculations, by setting the appropriate integration limits defined by the layer structure, the total per unit area electron concentration inside the gated barrier-layer $n_{s\_barrier}$ and the sheet carrier concentration in the underlying GaN channel n_{s_GaN} can be assessed individually, while n_{s_total} is the total electron concentration per unit area (i.e. calculated form the Schottky contact to the bottom of GaN buffer layer). The ratio of $n_{s\_barrier}$ to n_{s_GaN} offers a quantitative tool for assessing the degree of carrier spilling out of the GaN channel. In the evaluations presented here, the values of the threshold-voltage V_{th} of samples were calculated using linear extrapolation of n_{s_GaN} versus gate voltage (V_G). Figure 3.5 demonstrates the assessment of threshold-voltage in the specific case of a group 1 HFET. In evaluating the carrier confinement, since the value of V_{th} is varying among HFET of different layer structure and composition, the comparisons reported in this section were made while transistors were biased at different values of V_G yielding an identical value of n_{s_GaN}.

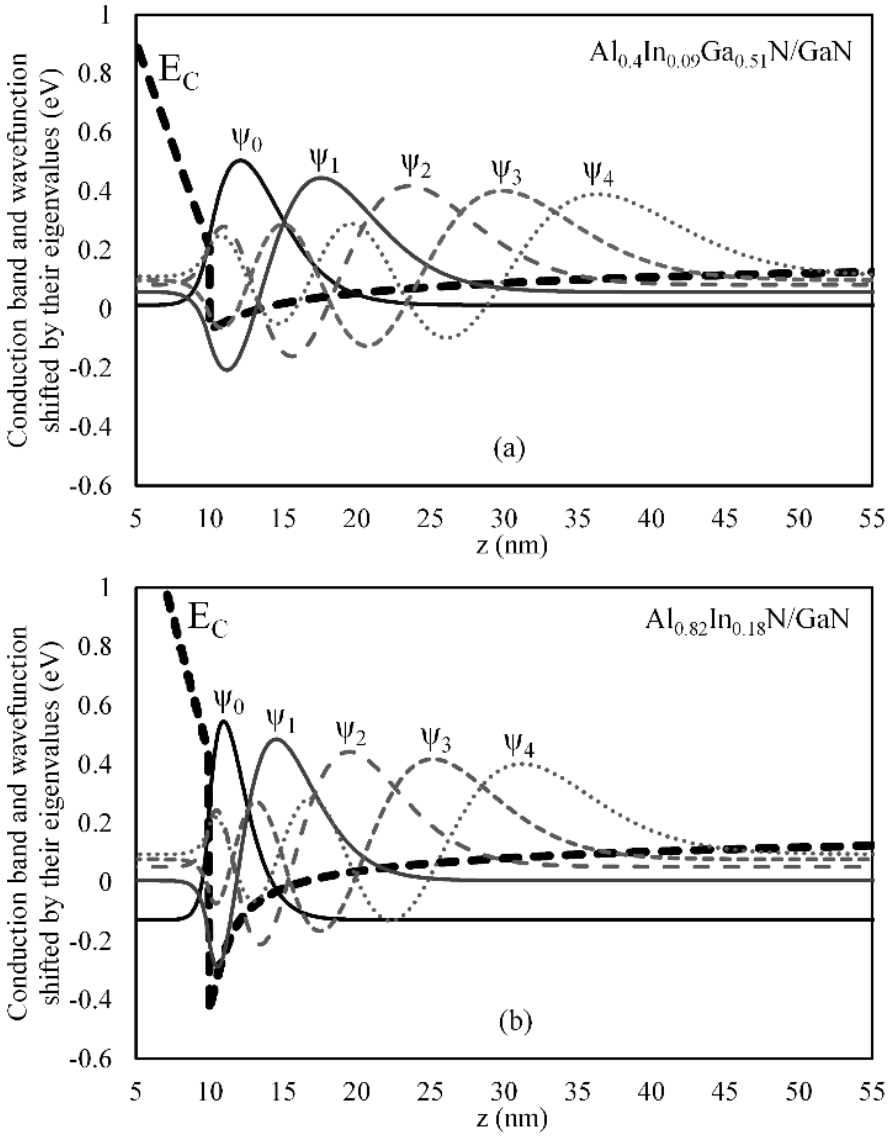


Figure 3.4 Computed wavefunctions of the first five subbands (ψ_0, ψ_1, ψ_2, ψ_3, and ψ_4) for (a) $Al_{0.4}In_{0.09}Ga_{0.51}N/GaN$, and (b) $Al_{0.82}In_{0.18}N/GaN$ HFETs at V_G=0 V. The wavefunctions are normalized to 1 $nm^{-1/2}$ and shifted by their eigenvalues.

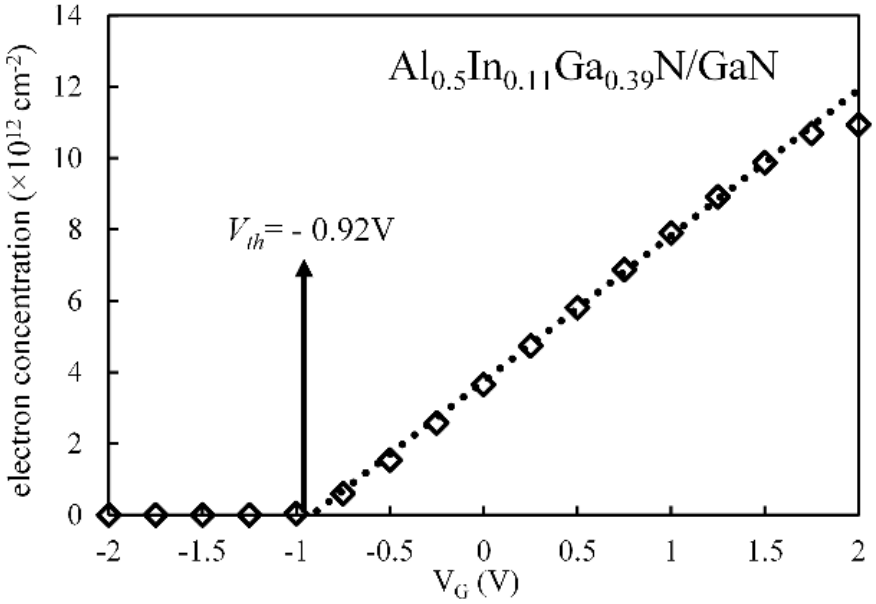


Figure 3.5 Calculation of the threshold-voltage based on the linear extrapolation of n_{s_GaN} versus V_G for $Al_{0.5}In_{0.11}Ga_{0.39}N$/GaN HFET.

Figure 3.6, as an example compares the electron concentrations calculated for two of the group 1 HFETs, while Table 3.1 summarizes $n_{s\_barrier}$, n_{s_GaN}, and n_{s_total} among the seven HFETs of this group. Based on the results presented in Fig. 3.6 and Table 3.1, corresponding to a lower carrier confinement, in the transistors with smaller ΔE_C and polarization, a larger portion of carriers spill into the barrier. Among the seven explored device varieties of this group, $Al_{0.2}In_{0.04}Ga_{0.76}N$/GaN with comparatively large positive V_{th} (which may be considered as a good choice for an enhancement-mode lattice-match quaternary HFET) shows a relatively poor carrier confinement with 18.55% of the carriers residing inside the barrier at a reasonable V_G of just about 0.95 V above V_{th}.

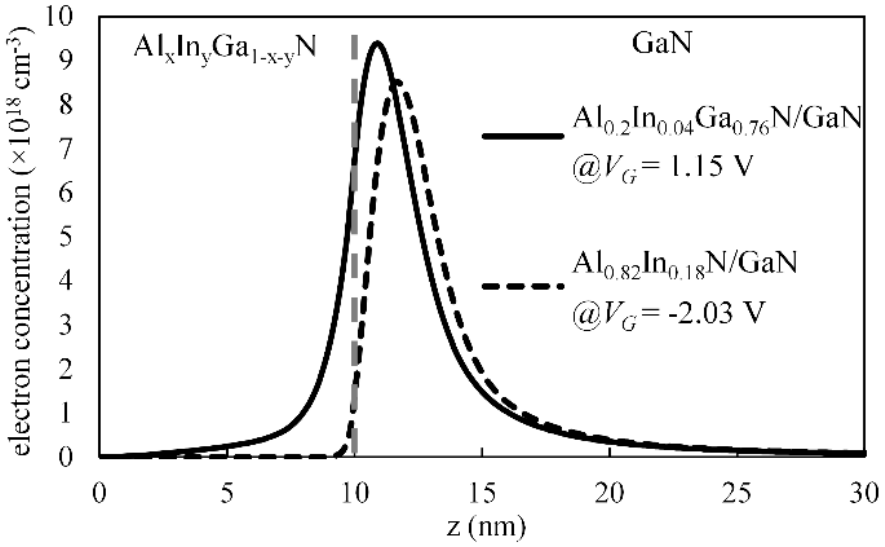


Figure 3.6. Electron concentration versus z under the gate of two HFETs of group 1 (i.e. with different metal mole-fractions of the barrier-layer). Since the two HFETs manifest different values of threshold-voltage, the comparison has been made while transistors are biased at different values of V_G yielding identical values of n_{s_GaN}.

Table 3.1 Threshold-voltage and electron concentration calculated in different parts of the gated layer structure for the HFETs of group 1.

	V_{th} (V)	V_G (V)	n_{s_GaN} (cm^{-2})	$n_{s\_barrier}$ (cm^{-2})	n_{s_total} (cm^{-2})	$n_{s\_barrier}/n_{s\_total}$ (%)
$Al_{0.2}In_{0.04}Ga_{0.76}N/GaN$	+0.20	1.15	3.42×10^{12}	7.79×10^{11}	4.2×10^{12}	18.55
$Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$	+0.02	0.92	3.42×10^{12}	3.14×10^{11}	3.74×10^{12}	8.40
$Al_{0.4}In_{0.09}Ga_{0.51}N/GaN$	-0.43	0.46	3.42×10^{12}	1.51×10^{11}	3.57×10^{12}	4.22
$Al_{0.5}In_{0.11}Ga_{0.39}N/GaN$	-0.92	-0.05	3.42×10^{12}	9.00×10^{10}	3.51×10^{12}	2.56
$Al_{0.6}In_{0.13}Ga_{0.27}N/GaN$	-1.48	-0.64	3.42×10^{12}	5.90×10^{10}	3.48×10^{12}	1.69
$Al_{0.7}In_{0.15}Ga_{0.15}N/GaN$	-2.11	-1.31	3.42×10^{12}	4.08×10^{10}	3.46×10^{12}	1.18
$Al_{0.82}In_{0.18}N/GaN$	-2.80	-2.03	3.42×10^{12}	2.87×10^{10}	3.45×10^{12}	0.83

Table 3.2 Threshold-voltage and electron concentration calculated in different parts of the gated layer structure for the HFETs of group 2.

	V_{th} (V)	V_G (V)	n_{s_GaN} (cm^{-2})	$n_{s\_barrier}$ (cm^{-2})	n_{s_total} (cm^{-2})	$n_{s\_barrier}/n_{s\_total}$ (%)
$Al_{0.2}In_{0.04}Ga_{0.76}N$/AlN/GaN	-0.98	0.73	7.58×10^{12}	3.34×10^{10}	7.62×10^{12}	0.44
$Al_{0.3}In_{0.07}Ga_{0.63}N$/AlN/GaN	-1.12	0.59	7.58×10^{12}	3.27×10^{10}	7.61×10^{12}	0.43
$Al_{0.4}In_{0.09}Ga_{0.51}N$/AlN/GaN	-1.51	0.21	7.58×10^{12}	3.33×10^{10}	7.62×10^{12}	0.44
$Al_{0.5}In_{0.11}Ga_{0.39}N$/AlN/GaN	-1.98	-0.24	7.58×10^{12}	3.39×10^{10}	7.62×10^{12}	0.44
$Al_{0.6}In_{0.13}Ga_{0.27}N$/AlN/GaN	-2.45	-0.76	7.58×10^{12}	3.46×10^{10}	7.62×10^{12}	0.45
$Al_{0.7}In_{0.15}Ga_{0.15}N$/AlN/GaN	-3.03	-1.36	7.58×10^{12}	3.54×10^{10}	7.62×10^{12}	0.46
$Al_{0.82}In_{0.18}N$/AlN/GaN	-3.67	-2.00	7.58×10^{12}	3.63×10^{10}	7.62×10^{12}	0.48

Table 3.3 Threshold-voltage and electron concentration calculated in different parts of the gated layer structure for the HFETs of group 3.

	V_{th} (V)	V_G (V)	n_{s_GaN} (cm^{-2})	$n_{s\_barrier}$ (cm^{-2})	n_{s_total} (cm^{-2})	$n_{s\_barrier}/n_{s\_total}$ (%)
$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N$/GaN	+0.14	1.02	3.42×10^{12}	3.28×10^{11}	3.75×10^{12}	8.75
$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.4}In_{0.09}Ga_{0.51}N$/GaN	+0.07	0.90	3.42×10^{12}	1.53×10^{11}	3.58×10^{12}	4.27
$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.5}In_{0.11}Ga_{0.39}N$/GaN	-0.05	0.78	3.42×10^{12}	9.02×10^{10}	3.51×10^{12}	2.57
$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.6}In_{0.13}Ga_{0.27}N$/GaN	-0.15	0.66	3.42×10^{12}	5.90×10^{10}	3.48×10^{12}	1.70
$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.7}In_{0.15}Ga_{0.15}N$/GaN	-0.28	0.52	3.42×10^{12}	4.08×10^{10}	3.46×10^{12}	1.18
$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.82}In_{0.18}N$/GaN	-0.41	0.38	3.42×10^{12}	2.87×10^{10}	3.45×10^{12}	0.83

As mentioned earlier, a common method to shift the peak of the electron concentration away from the hetero-interface (and to enhance the carrier confinement) in AlGaN/GaN HFETs is to employ an AlN spacer layer [56]. While the use of such a spacer in the case of AlInGaN/GaN HFETs has been also reported [22],[33],[51]-[53], as shown in Table 3-2 such a choice seems counterintuitive. Table 3-2 presents the electron concentration across different regions of the seven indicated gated epilayers of group 2. According to this table, although employing a 1 nm thick AlN spacer layer considerably improves the carrier confinement, V_{th} of the devices of group 2 are observed to be considerably negative-shifted. This amount of shift prevents the lattice-match AlInGaN/GaN HFETs to realize an

enhancement-mode operation, unless employing a thinner overall barrier. Thinning of the barrier, since adding to the problem of gate leakage, is however not a very viable solution. Since compared to group 1 HFETs, group 2 HFETs manifest larger values of polarization induced sheet charge density at the hetero-interface, the collective n_{s_GaN} presented in Table 3-2 is comparatively larger than the one in Table 3-1.

Based on the above observation of the substantial impact of the largely lattice-mismatched AlN spacer layer of considerable spontaneous polarization mismatch to GaN in negating the gains of the lattice-match epilayers for achieving enhancement-mode operation, an epilayers design relying on the use of a lattice-match bilayer barrier was considered (group 3). Among these epilayers, in order to achieve the best possible carrier confinement while a V_{th} compatible with the enhancement-mode operation is sustained, the metal mole-fractions of the 8 nm thick $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N$ barrier layer was chosen for minimization of the spontaneous polarization difference to the GaN channel, while the 2 nm thick $Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$ spacer layer was selected with the goal of achieving the largest possible conduction-band discontinuity to GaN. Since both AlInGaN layers are lattice-match to GaN, no piezoelectric effect exists at the hetero-interfaces. In this design, the effect of larger spontaneous polarization mismatch between the $Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$ spacer layer and GaN becomes less consequential for spacers of smaller thickness.

As an example among group 3 HFETs, Fig. 3.7 presents the thermal-equilibrium conduction-band diagram and n_s versus z for a gated $Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ HFET. As indicated in this figure, in this layer structure two sheets of polarization-induced charge are present at the

$Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N$ and the $Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ hetero-interfaces (σ_1 and σ_2, respectively). σ_1 and σ_2 can be calculated as:

$$\sigma_1 = P_{SP}\left(Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N\right) - P_{SP}\left(Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N\right), \quad (3.1)$$

$$\sigma_2 = P_{SP}\left(Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N\right) - P_{SP}(GaN), \quad (3.2)$$

in which, $P_{SP}(Al_xIn_yGa_{1-x-y}N)$ and $P_{SP}(GaN)$ are the spontaneous polarization of the quaternary $Al_xIn_yGa_{1-x-y}N$ barrier-layer and GaN, respectively. The foundation of the calculation framework of spontaneous polarization among quaternary layers has been previously discussed in chapter 2.

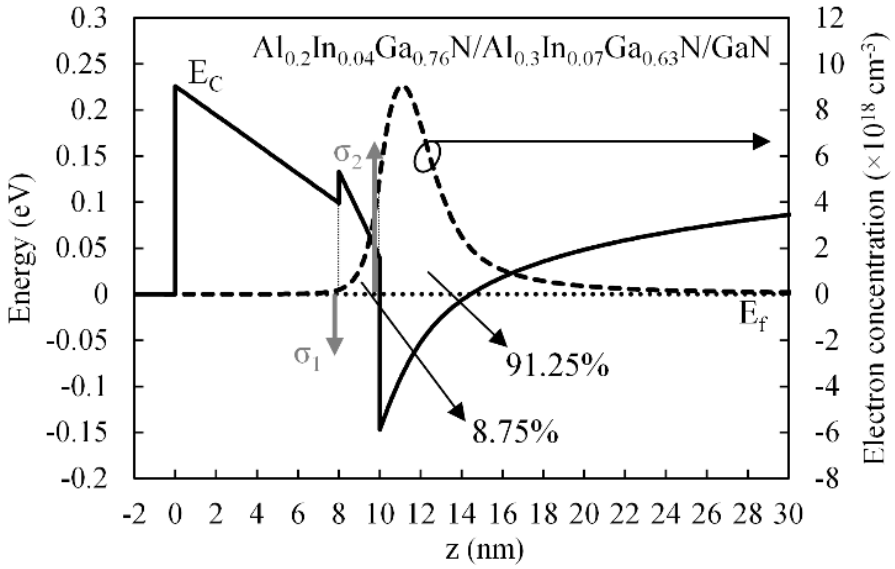


Figure 3.7 Thermal-equilibrium conduction-band diagram and n_s versus z for the Ni-gated $Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$. σ_1=-0.36 μC/cm^2 and σ_2=1.05 μC/cm^2 are the polarization-induced sheet charge densities at $Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N$ and $Al_{0.3}In_{0.07}Ga_{0.63}N/GaN$ hetero-interfaces, respectively. Threshold-voltage has been calculated as +0.14 V and $n_{s\_barrier}/n_{s\_total}$ is 8.75% for this HFET at V_G=1.02 V.

According to the strategy highlighted above, Table 3.3 summarizes V_{th} and the electron concentration in different regions of the gated epilayers of group 3 HFETs. These HFETs were considered according to the best choice of metal mole-fractions for barrier layer

among the seven points identified on Fig. 3.2 (i.e. x_1=0.2 and y_1=0.04). As quantitatively affirmed in Table 3.1, in the selection of metal mole fractions of $Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$ spacer layer, not only the larger ΔE_C but also the enhanced polarization-induced charge density at $Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$/GaN hetero-interface ($\sigma_2$) lead to the better carrier confinement. However, this choice also causes a negative-shift in V_{th}. Reducing the thickness of $Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$ spacer layer can help with positive shifting the V_{th}, as σ_1 and σ_2 approach each other. However, thinning the spacer layer is limited by the alloyed nature of this layer. In this study, the thickness of the spacer layer has been considered as 2 nm, which is almost six times the lattice constant.

Comparing the data presented in Tables 3.1, 3.2, and 3.3, it can be concluded that in comparison to the conventional lattice-match $Al_xIn_yGa_{1-x-y}N$/GaN HFETs, employing a bilayer lattice-match spacer/barrier offers a substantial improvement to carrier confinement in the enhancement-mode HFET (i.e. by about 10 percent at 1 V of gate overdrive), while imposing very little negative shift on V_{th}. The expected gain in carrier confinement by adopting the group 3 design strategy is expected to be further improved at higher gate overdrives. As a result of these observations, on the balance of the indicated factors, the proposed layer structure seems to offer the most viable solution for achieving enhancement-mode operation in the lattice-match GaN-channel transistors. While in comparison to group 2, group 3 transistors are expected to suffer more from remote alloy scattering, the elimination of piezoelectric effect and better confinement of electrons to the higher mobility GaN channel is expected to offer these transistors a superb current drive in the enhancement-mode operation.

3.4 Conclusion

Based on the simulations performed using the commercial Poisson-Schrödinger solver *Nextnano*, a quaternary lattice-match AlInGaN bilayer barrier/spacer design for GaN-channel HFETs was presented. Accordingly, it was shown that this layer structure has the possibility of offering enhancement-mode operation, while allowing good carrier confinement at substantial gate overdrives. Since the proposed barrier/spacer stack is fully lattice-match to the GaN channel, it also allows for relieving some of the difficulties often attributed to strain relaxation and long term reliability of these polar III-nitride hetero-structures.

Chapter 4

Modeling of Gate leakage in GaN-channel HFETs

The contributions of this chapter have been already published [57][1]. Most of the materials are taken from Ref. [57] and an under-review manuscript mentioned in chapter 1.

4.1 Introduction

In spite of the larger Schottky barrier-height, reverse gate-current of GaN-channel HFETs has been so far observed to remain at higher levels compared to the AlGaAs/GaAs counterparts [9]-[11]. The higher leakage is usually attributed to the high density of traps residing within the AlGaN barrier [9]-[20]. Over the past two decades, a number of models relying on mechanisms such as multistep tunneling through the AlGaN barrier, also known as trap-assisted tunneling (TAT) [9], [10], [12], and Poole-Frenkel (PF) leakage through a continuum of trap states in the barrier have been proposed [13]-[18]. These mechanisms are believed to be the dominant leakage processes for moderate values of temperature and gate-source bias.

In addition, gate-leakage in AlGaN/GaN HFETs has been sometimes observed to take a one step tunneling approach. When the electric-field across the barrier is strong enough,

[1] - In [57], Dr. Pouya Valizadeh was the supervisor, and the rest of work were contributions of Hassan Rahbardar Mojaver.

Fowler-Nordheim tunneling (FN) across the barrier is often detected [19], while when the electron-temperature is moderately elevated thermionic field-emission (TFE) takes over. There are also some studies on surface leakage in the form of hopping through surface traps from the gate to the source and drain contacts [20]. This current component can become significant at large gate-source or gate-drain biases.

Temperature- or bias-dependence of these leakage mechanisms can be used to distinguish between the aforementioned culprits. Since depending on a set of deterministic parameters (i.e. Schottky barrier-height, electric-field, and temperature), among these processes FN and TFE are easier to be recognized. However, due to the strong dependence on trap characteristics, the choice of parameters used in TAT and PF is not as straightforward.

In the study presented in this chapter, temperature- and bias-dependent study of the gate-current in a group of devices built on alternative isolation-feature geometries is performed. Details of the fabrication process of these devices which offer a larger number of gate-covered sidewalls can be found in [58]. For each isolation-feature geometry the gate-current studies reveal a correlation between the gate-current and the number of gate-covered sidewalls. Uncorrelated to the aforementioned leakage mechanisms, this observation provides evidence into the existence of a leakage path between the two-dimensional electron gas (2DEG) and the gate-metal. Although this has been already identified as a leakage path in Schottky test structures made on AlGaN/GaN epilayers [59], and also in a few transistors such as GaInP/InGaAs [60], and InAlAs/InGaAs HFETs [61], [62], its relevance to modeling the gate-leakage of AlGaN/GaN HFETs and its voltage and temperature dependence have attracted limited attention [63]-[65].

Following the observation of this leakage path, in an attempt to outline a model with

realistic set of assumption for describing the reverse gate-current of GaN-channel HFETs, in addition to the leakage taking place through the III-Nitride barrier, the path via the mesa sidewalls is considered. To assess the validity of the assumptions, and to determine the dominant electron transport mechanism in each identified path, temperature- and bias-dependence of the assumed electron transport processes are analyzed. In case of FN, the previously reported inconsistencies in adopting the constants of the model are also thoroughly discussed [13].

4.2 Leakage via the AlGaN barrier and conduction through the mesa sidewalls

In an attempt to investigate the contributions of the gate-covered mesa-sidewalls to the gate-current of AlGaN/GaN HFETs, the V_{GS}-dependence of this current component is studied across a number of devices built on a few alternative isolation-features (instead of the regular cubic mesa). The structures of these devices are depicted in Fig. 4.1. All these devices were built on an epitaxial layer structure consisting of a 20 nm thick unintentionally doped (UID) $Al_{0.3}Ga_{0.7}N$ barrier, a 1 nm thick AlN spacer, and a UID GaN channel followed by the Fe-doped GaN buffer layer. Further details of the fabrication process can be found in [58]. Figure 4.2 provides gate-dissected cross-sectional views of the fin, 7-island, and 14-island device varieties with indication of the size of the important dimensions. Based on the structures presented in Fig. 4.1, since the likewise defined cross-sectional views are identical in case of the 14-island, comb, ladder, and inverted-fin structures, the 14-island is taken as a representative. As shown in Fig. 4.2, all of the investigated transistors share an almost equal value of gate-width.

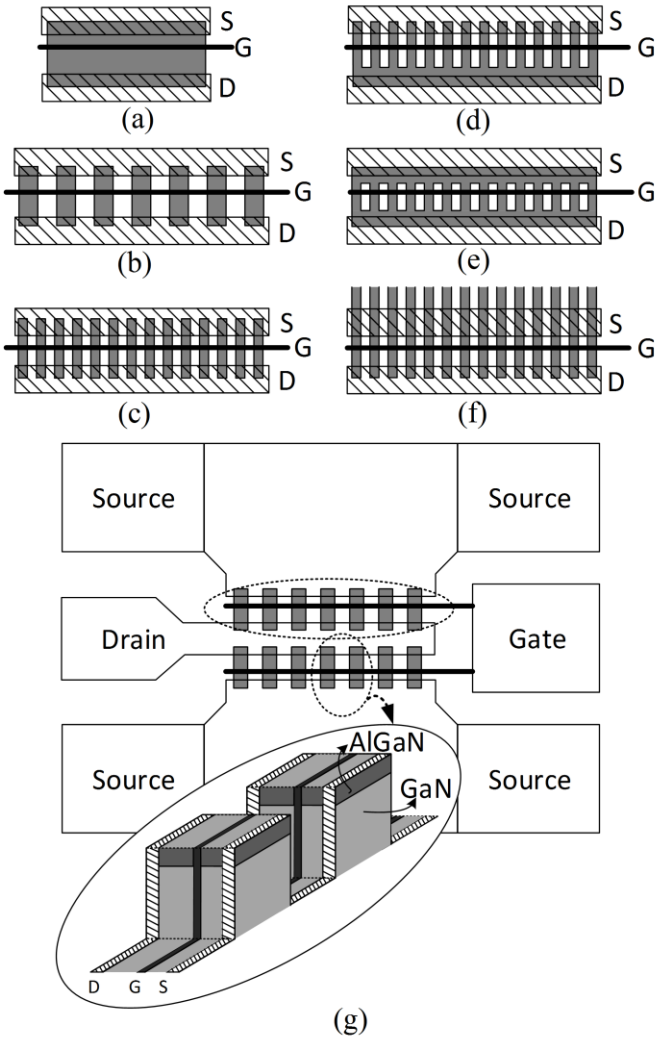


Figure 4.1 (a)-(f) represent the top views of devices built on isolation-features known as: fin, 7-island, 14-island, comb, ladder, and inverted-fin, respectively. In case of the inverted-fin, only the widths of the fins within the proximity of one gate finger are shown. The gray areas on these top views represent the surface of each isolation-feature resulting from etching of the AlGaN/AlN/GaN structure to a 300 nm depth. The aforementioned names are illustrative of these shapes. Among these figures, the hash-marked areas represent the ohmic contact of source and drain, and the black lines stand for gate-fingers. (g) represents the complete top view of a two-finger HFET with the depiction of contact pads in case of the 7-island structure represented in (b).The inset shows the 3D schematic in case of two of the islands. The area marked by the larger dotted oval is the area presented in (b). Gate-source spacing and gate-drain spacing are 2 μm and 4 μm, respectively, while gate length (L_G) was either 0.5 μm or 1 μm.

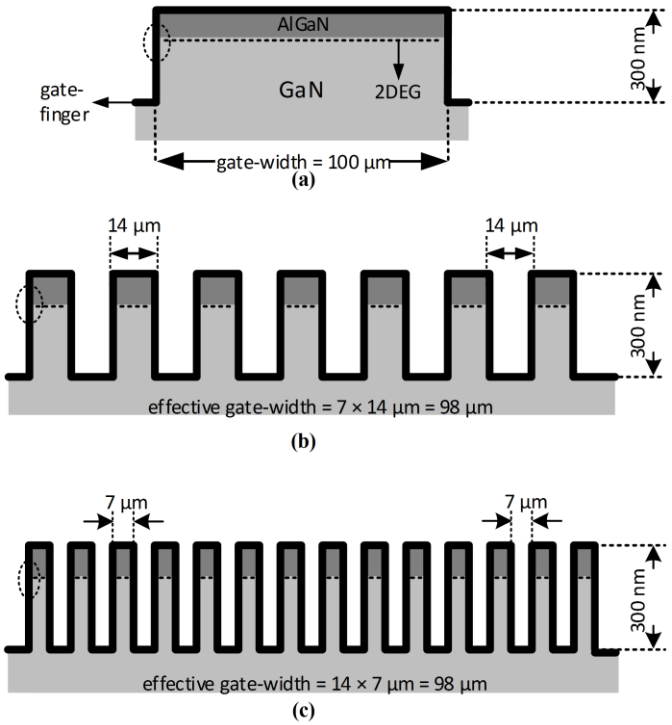


Figure 4.2 Gate-dissected cross-sectional views of the fin (a), 7-island (b), and 14-island (c) device varieties with indication of the size of the important dimensions. The cross-sectional views are provided in planes parallel with the gate-finger. The heights of the features are not drawn to scale. The color code of the layer structure expressed in (a) is also applicable to (b) and (c). In each case, as an example on one of the gate-covered sidewalls the point of overlap of the gate-finger and the 2DEG is identified by the dashed oval.

Figure 4.3 provides plots of the room-temperature measured I_G for the transistors depicted in Fig. 4.1. Among these plots, for large negative values of V_{GS}, there is no tangible difference among the reported values of I_G. Thus, the common phenomenon of leakage through the equally wide barrier is expected to be responsible for the gate current. For less negative values of V_{GS}, disappearance of this observation among the devices having unequal number of gate-overlaps with the 2DEG at the sidewalls of the isolation-feature heralds the beginning of an excess-leakage regime. As observed on this figure, the gate-current among the 14-island, ladder, comb, and the inverted-fin structures remains identical even under the excess-leakage regime. However, the gate of the 7-island and fin-isolated devices

demonstrate more than one order of magnitude less leakage than these groups of devices. Based on the almost equal values of the effective gate-width among all of the aforementioned transistor varieties (from 98 to 100 μm), the sizeable difference between the values of I_G identifies a leakage path unrelated to the size of the gate-overlapped top surface of the isolation-feature. Hence, the excess leakage is expected to be unrelated to leakage through the AlGaN barrier in a path normal to the hetero-interface.

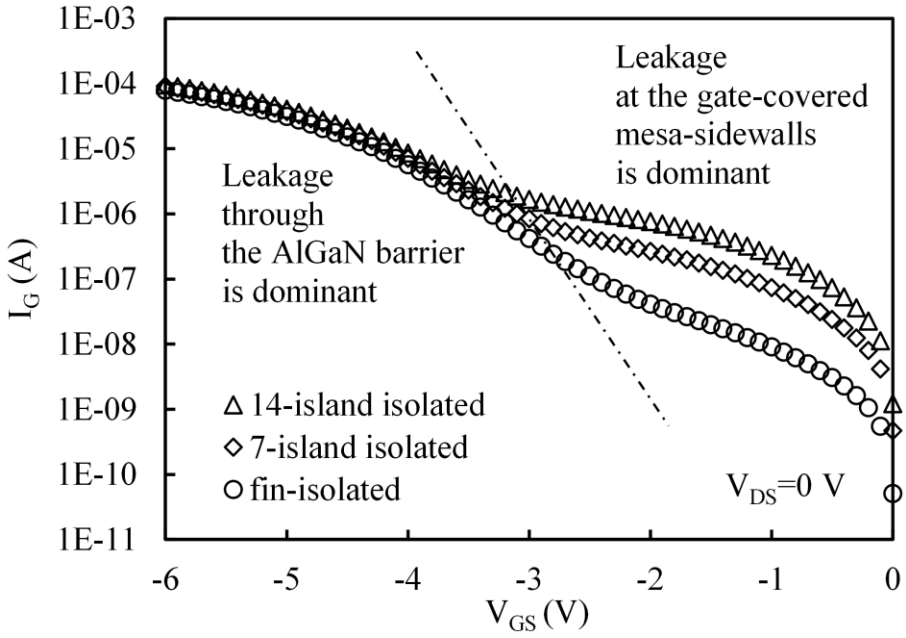


Figure 4.3 Measured I_G versus V_{GS} for the devices built on the six different isolation-feature geometries presented in Fig. 4.1. The lowest and the middle sets of data points are associated with fin and 7-island isolation-feature geometries, respectively. Data points for 14-island, comb, ladder, and inverted-fin consisting of 14 individual features interfacing the gate finger exactly coincide with one another. Thus, the 14-island is taken as a representative. Measurements were performed at room temperature. L_G is 0.5 μm.

A seemingly responsible explanation for this observation can be sought in the difference between the surface components of gate-leakage when the transistor is realized on an isolation-feature with a footprint wider than the effective gate-width. However, considering the fact that the isolation-feature height is only 300 nm, this explanation is deemed incapable of yielding an answer to the orders of magnitude difference in I_G. This is since

the difference in the overall surface area at the source and drain access-regions among all devices varieties is negligible. This argument is further supported by the similarity of the gate-leakage among the ladder and 14-island device varieties. According to Fig. 4.1, among these two groups although the latter presents drain and source access-regions on the sidewalls of the features and on the etched GaN surface, in the former group such regions are only formed on the AlGaN surface. The explanation based on the variation of the surface-component of gate-leakage is even less likely to hold when considering the fact that all exposed surfaces of these devices were passivated with a SiN_x film, which has been reported to reduce the surface leakage at least by two orders of magnitude [66]. Success of the surface passivation process was assessed by the lack of observation of gate-lag, and frequency dispersion on drain-current and gate-transconductance of all device varieties.

4.3 Determination of the dominant electron transport mechanism

Formulating a gate-current model, considering the two main recognized paths of leakage, (i.e. the leakage through the AlGaN barrier and the leakage through the mesa sidewalls), requires the identification of the dominant transport mechanism across each path. In this section, relying on the experimental data from the devices mentioned in section 4.2, and a few published sets of data, it is attempted to present a realistic assessment of the dominant transport processes.

4.3.1 The dominant leakage mechanism through the polar III-Nitride barrier

For large negative values of V_{GS}, due to the presence of strong electric field across the barrier, the FN tunneling process through the barrier has been deemed the most probable

contributor to I_G [19], . While there is consensus on this matter, often in formulating the current density according to this process unrealistic assumptions about certain constants seem inevitable. The FN current density is given by [13], [67]

$$J_{FN} = AE^2 \exp\left(-\frac{8\pi\sqrt{2m_n^* q}}{3hE}\phi_b^{3/2}\right) \tag{4.1}$$

for $A = \frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$ in which, q is the fundamental electronic charge, h is Planck's constant, m_0 is the free-electron mass, m_n^* is the conduction-band effective mass in the barrier layer, $q\phi_b$ is the Schottky barrier height, and E is the electric field across the barrier. Assuming a triangular approximation for the shape of the polar III-Nitride barrier, electric field E is approximately given by [9],

$$E = \frac{\phi_b - V_{GS} - (\Delta E_c/q) + \phi_F}{d_{barrier}} \qquad \text{for } V_{GS} > V_{th} \tag{4.2}$$

in which, ΔE_c is the conduction-band offset at the barrier/channel hetero-interface, $q\phi_F$ is the difference between fermi energy level and conduction-band edge at the GaN side, $d_{barrier}$ is the barrier thickness, and V_{th} is the threshold-voltage of the HFET. For the fin variety of the AlGaN/GaN HFETs discussed in section 4.2, V_{th} is about -4.5. Due to depletion of the 2DEG at gate-source biases lower than the threshold-voltage, the electric field across the barrier becomes independent of V_{GS}. Although ϕ_F is a function of V_{GS} [34], for values of V_{GS} close to V_{th} (when the higher subbands are not populated) it can be assumed to remain unchanged with bias. Coincidently, as marked in Fig. 4.3 for the group of polar AlGaN/GaN HFETs, this is the regime where leakage through the barrier becomes dominant.

According to (4.1), the linear dependence of $\ln(J/E^2)$ vs. $1/E$ is counted as an evidence of the dominant presence of FN tunneling [11], [13], [16], [19], [67]. Therefore, the slope of this linear characteristic is expected to be proportional to $\sqrt{m_n^*}\phi_b^{3/2}$, while its intercept with the vertical axis is defined in terms of $m_n^*\phi_b$. However, for both polar AlGaN/GaN and InAlN/GaN HFETs extraction of the values of m_n^* and ϕ_b through modeling the experimentally recorded FN-dominated gate-current has resulted in evident inconsistencies [11], [13], [16], [68], [69]. In order to assess the cause(s) of this problem, in addition to the data gathered from the fin variety of the devices identified in section 4.2, measurements reported in three representative studies on FN-dominated I_G in AlGaN/GaN and lattice-match InAlN/GaN HFETs are scrutinized [11], [13], [16]. Figure 4.4 presents the linear region of $\ln(J_G/E^2)$ vs. $1/E$ for the mentioned studies, where J_G is the gate-current density. Specifications of the barrier layer in each of these studies, along with the extracted (or adopted) values of m_n^* and $q\phi_b$ from Fig. 4.4 are presented in Table 4.1.

For a 25 nm thick barrier in an $Al_{0.25}Ga_{0.75}N$/GaN HFET, Zhang *et al.* assumed $q\phi_b$ of 1.17 eV (which is in agreement with the typically estimated values [8]), and according to the slope of the linear characteristics reproduced in Fig. 4.4(a) extracted the value of m_n^* to be equal to $0.0016m_0$ [13]. As it has been also noted in [13], this extracted value of the effective-mass is much smaller than the typically measured or estimated value of around $0.4m_0$ for $Al_{0.25}Ga_{0.75}N$ [13], [70]. For these parameters, in case of [13] the extracted value of the y-intercept in Fig. 4.4(a) is considerably different from the value expected from (4.1). As indicated in Table 4.1, this value presented as the ratio of A to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$ is 6.04×10^{-11}. This implies that taking the aforementioned values of m_n^* and $q\phi_b$,

the expected current density generated by the FN tunneling through the barrier is more than 10 orders of magnitude larger than the measured value (expressed in terms of A).

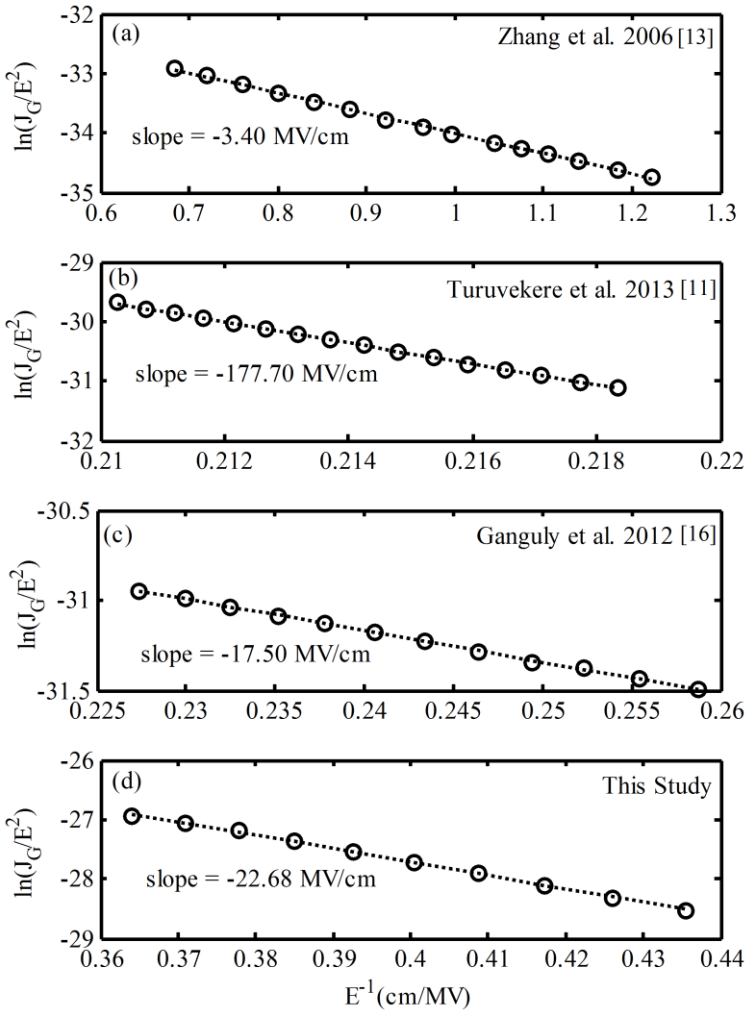


Figure 4.4 (a), (b), and (c), show the $\ln(J_G/E^2)$ vs. $1/E$ data collected from [13], [11], [16], respectively. The data from the fin-isolated devices of 0.5 μm gate-length of the present study are given in (d). Symbols represent the experimentally acquired data points and the dotted lines illustrate the linear interpolation among these points

Table 4.1 Barrier structure and the adopted/extracted parameters for the observed FN leakage through the barrier.

Barrier Structure	$q\phi_b$ (eV)	m_n^*/m_0	Ratio of the extracted value of A in (1) to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$	Ref.
$Al_{0.25}Ga_{0.75}N$ 25nm	1.17(a)	0.0016(e)	6.04×10^{-11}	[13]
$In_{0.17}Al_{0.83}N$/ AlN	2.56(e)	0.4(a)	1.15×10^{9}	[11]
$In_{0.17}Al_{0.83}N$/ AlN	0.7(e)	0.2(a)	1.74×10^{-7}	[16]
$Al_{0.3}Ga_{0.7}N$/AlN 20nm/1nm	1.23(a)	0.0593(e)	3.80×10^{-4}	This study[1]
$Al_{0.3}Ga_{0.7}N$/AlN 20nm/1nm	1.23(a)	0.4(e)	3.80×10^{-4}	This study[2]

[1]Considering E as estimated by (4.2).
[2]Considering E as 2.60 times of the value estimated by (4.2).
Superscripts (a) and (e) stand for adopted and extracted, respectively.

In case of a lattice-match $In_{0.17}Al_{0.83}N$/GaN HFET, Turuvekere *et al.* assumed $m_n^* = 0.4m_0$ and extracted $q\phi_b = 2.56eV$ from the slope of the linear characteristics reproduced in Fig. 4.4(b) [11]. Whereas the value of the Schottky barrier height is larger than the 1.46 eV reported for Ni/InAlN [71], the assumed value of the conduction-band effective mass in $In_{0.17}Al_{0.83}N$ is still within the acceptable range. Nonetheless, the extracted value of the y-intercept in Fig. 4.4(b) is still considerably different from the value expected from (4.1). In this case, as indicated in Table 4.1, the expected current density generated by the FN tunneling through the barrier is about 9 orders of magnitude smaller than the measured value.

Also in case of a lattice-match $In_{0.17}Al_{0.83}N$/GaN HFET, assuming the reasonable value of $m_n^* = 0.2m_0$ [70], Ganguly *et al.* extracted $q\phi_b = 0.7eV$ based on the linear characteristics reproduced in Fig. 4.4(c) [16]. This lower than expected value of the Schottky barrier height is speculated to be due to microscopic In-composition fluctuations

in the InAlN barrier [16]. Although not explicitly expressed in [16], the extracted value of y-intercept in Fig. 4.2(c) is still considerably different from the value expected from (4.1). In this case, as indicated in Table 4.1, the expected current density generated by the FN tunneling through the barrier is about 6 orders of magnitude larger than the measured value (expressed in terms of *A*). According to the aforementioned reference in [16] to the possibility of composition fluctuation in the barrier, as long as the expected I_G is greater than the measured value (i.e. unlike [11]), this observation can be attributed to the possibility of a relatively small fraction of the surface of the barrier (associated with high In-composition) being responsible for FN tunneling.

For the AlGaN/GaN HFETs mentioned in section 4.2, assuming the typical value of 1.23 eV of $q\phi_b$ for the Ni gate [8], based on the slope of the FN characteristics of gate-leakage presented in Fig. 4.4(d), the value of m_n^* is extracted as $0.0593m_0$. In this case, as indicated in Table 4.1, the expected current density generated by the FN tunneling through the barrier is about 3 orders of magnitude larger than the measured value (expressed in terms of *A*).

In each of the above mentioned cases, there exists a correlation between the two observed discrepancies (i.e. of the vertical axis intercept and the required value of the effective mass). A seemingly reasonable explanation for these observations lies in the presence of the exponential term in (4.1). While J_{FN} dramatically changes with $q\phi_b$ and *E*, the presence of a degree of non-uniformity across the surface allows the electric field and the Schottky barrier height to be position dependent. Accordingly, the FN tunneling through a part of barrier which boasts smaller $q\phi_b$ and/or larger *E* can dominate the total current density. This portion of the surface of the barrier can be referred to as *"FN leakage zone"*. While the proportion of the total area responsible for FN gate-leakage presents a chance for

explaining the smaller than 1 values of the ratio of the extracted value of A in (4.1) to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$ (presented in Table 4.1), the corresponding number greater than 1 which was reported from [11] remains puzzling. Table 4.1 also presents an example on the role of E in assessing the effective electron mass in case of the devices mentioned in section 4.2. According to the data presented in final row of this table, if the electric field were assumed to be almost 2.6 times as strong as the value calculated by (4.2), both $q\phi_b$ and m_n^* will take realistic values. In this case, if the *FN leakage zone* takes on only 0.038 percent of the gated surface area, not only the discrepancy on the effective mass but also on the readout of the y-intercept will be eliminated.

The answer to the question on whether FN leakage zone in a particular HFET is attributed to a higher E or a smaller $q\phi_b$ (or both) depends on the physical and compositional characteristics of the barrier. Due to the high possibility of In desorption (and In fluctuation) in the growth of In containing barriers of lattice-match InAlN/GaN HFETs [72], [73], formation of a FN leakage zone can be more readily attributed to a lower than expected value of $q\phi_b$. This is in agreement with the abovementioned speculations of [16]. In an attempt to substantiate the proposal on the existence of a *FN leakage zone*, the gate-currents among two groups of fin-type devices with the gate length of 0.5 and 1 μm have been compared. Both groups share the same value of gate width, as indicated in section 4.2. Results are presented in Fig. 4.5. According to this figure, both groups of HFETs present almost the same amount of gate-leakage (i.e. independent of 100 percent increase in the area of the gate electrode). This observation corroborates the proposed hypothesis of the existence of a FN leakage zone, according to which the whole gate area is not considered to be involved in the FN process. Further to this point, if the fluctuation of Ga

composition in the barrier was responsible for the higher leakage in *FN leakage zone*, assuming the almost uniform distribution of points of higher Ga composition, the HFET with larger gate area should have presented an almost twice as high of I_G. Accordingly, for the AlGaN/GaN HFETs used in this study the *FN leakage zone* should be seemingly attributed to the parts of barrier boasting higher values of electric field. Since according to Fig. 4.5, the area of the proposed *FN leakage zone* does not change considerably with the 100 percent increase of the total gate area, in correlation with a negligible increase in the perimeter of this gate covered area the expected region of higher *E* can be attributed to this periphery. Barrier thinning due to the presence of surface defects can be one of the reasons for the generation of FN leakage zone [74]. As mentioned earlier, in the final row of Table 4.1 such an impact has been considered in terms of an electric field 2.6 times as strong as expected from (4.2). In the remainder of the manuscript, this ratio is expressed by γ.

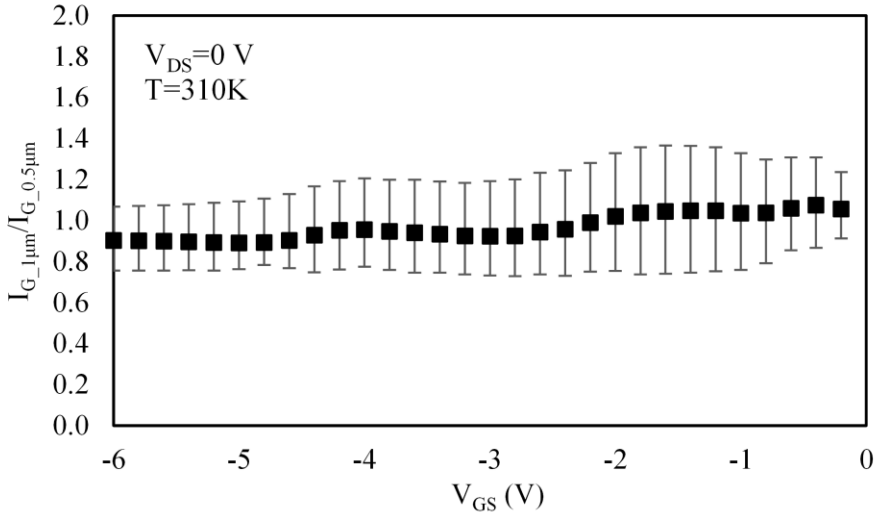


Figure 4.5 The ratio of gate current among two groups of fin-type similar HFETs with the gate length of 0.5 and 1 μm. Rectangular symbols represent the average of experimental data points while the bars provide the range of variation among a large number of identical devices.

While the hypothesis on the existence of a *FN leakage zone* in the gate-covered periphery of the isolation-feature seems to provide reasonable evidence on the dominance of FN process (i.e. when a large negative V_{GS} is applied) without any need for invoking unreasonable assumptions, the dominance of FN is still needed to be substantiated via studying the temperature dependence of the I_G. In spite of the temperature independence of quantum tunneling, the temperature dependence of the concentration of impinging charge carriers is still responsible for making the FN process a function of temperature [67]. This effect is modeled by incorporating a multiplicative term of $\pi ckT/\sin(\pi ckT)$ in (4.1), in which k is the Boltzmann constant, T is the temperature in Kelvin and c is defined as:

$$c = \frac{4\pi\sqrt{2m_n^*\phi_b}}{hE}. \tag{4.3}$$

The existence of E in the definition of c has a negligible impact on the linear characteristics reported in Fig. 4.4. Considering the effect of temperature on $q\phi_b$ and the barrier-lowering due to presence of image forces at the metal-barrier contact, $q\phi_b$ can be represented by [75], [76],

$$q\phi_b = q\phi_{b0} - \frac{\alpha T^2}{\beta + T} - \sqrt{\frac{q^3 E}{4\pi\varepsilon_r\varepsilon_0}} \tag{4.4}$$

in which, α is the Varshni empirical constant, β is a constant defined in close association with the Debye temperature, and ϕ_{b0} is selected in a way that at T = 300K and zero E, $q\phi_b$ reaches the typical value mentioned in [8] as a function of the Al composition. ε_0 is the permittivity of vacuum, and ε_r is the relative permittivity of the barrier. Applying these

factors, in order to explain the temperature dependence of the FN process, (4.1) is modified to,

$$I_{FN} = S_{FN} \frac{q^2(m_0/m_n^*)}{8\pi h\phi_b} \frac{\pi ckT}{\sin(\pi ckT)} (\gamma E)^2 \times \exp\left(-\frac{8\pi\sqrt{2m_n^* q}}{3h\gamma E}\phi_b^{3/2}\right) \quad (4.5)$$

where S_{FN} stands for the area of the *FN leakage zone*.

Figure 4.6 presents $\ln(I_G/E^2)$ vs. $1/E$ for the AlGaN/GaN HFETs identified in section 4.2 over a wide range of temperature. The room-temperature value of the parameters taken into account for presenting the data points of Fig. 4.6 in term of (4.5) are summarized in Table 4.2. As shown in Fig. 4.6, these same values have been proven to be well suited to express the value of I_G at other temperatures from 150 to 470 K.

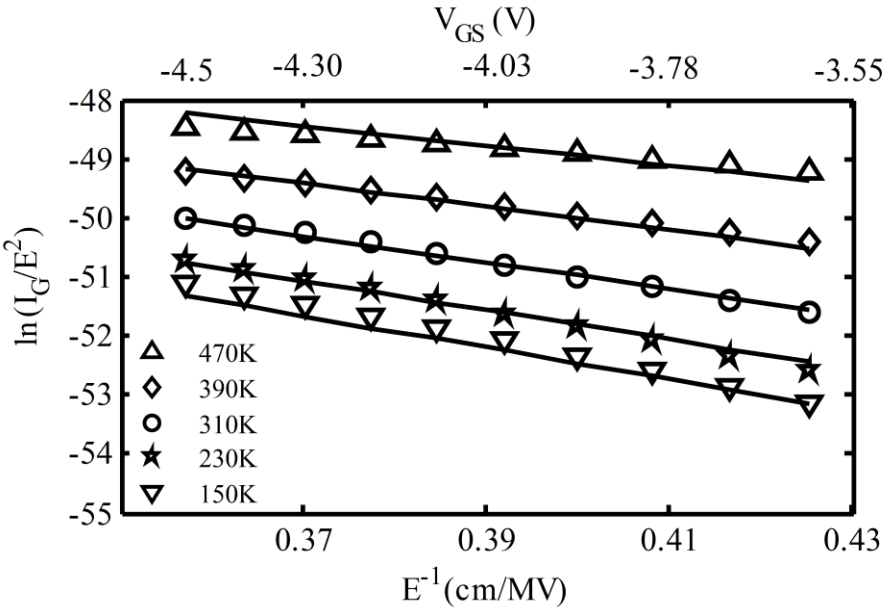


Figure 4.6 $\ln(I_G/E^2)$ vs. E^{-1} over wide range of temperature and when FN is dominant. Symbols represent experimental data points. Curves present the calculated values on the assumption of (4.5). V_{DS} is equal to 0 V. L_G is 0.5 µm.

Table 4.2 Parameters used in expressing the Fowler Nordheim tunneling current through the barrier of aluminum composition of 0.3

Sym.	*Definition*	*Value*	*Unit*	Ref.
ϕ_b at T=300 K, E=0 V/m	Ni/barrier Schottky barrier height	1.23	eV	[8]
m_n^*	Conduction-band effective mass in $Al_{0.3}Ga_{0.7}N$	$0.4 \times 9.11 \times 10^{-31}$	kg	[70]
α	Varshni empirical constant	1.4	meV/K	[77], [78]
β	Constant defined in association with the Debye temperature	860	K	[77], [78]
ε_r	relative dielectric constant	10.31	---	[8]
γ	Magnification of *E* across the FN leakage zone	1.8039	---	Extracted
S_{FN}	FN leakage zone area	6.02×10^{-14}	m^2	Extracted

4.3.2 Dominant leakage mechanism at gate-covered mesa sidewalls

Whereas the FN based model presented in the previous section seems capable of accurately forecasting the amount of gate-leakage for more negative values of V_{GS}, as highlighted in Fig. 4.3 for values of V_{GS} closer to 0 V existence of a certain correlation with the number of gate-covered sidewalls rules out the dominance of FN. For this latter range of V_{GS}, the study of temperature dependence of Pool-Frenkel (PF) electron emission taking place between the gate-covering mesa sidewall and the 2DEG among the AlGaN/GaN HFETs mentioned in section 4.2 seems to provide sufficient evidence on the dominance of this mechanism. It has to be highlighted that due to the presence of fermi-level pinning at the non-polar III-Nitride surfaces [79], and also barrier thinning at these sidewalls (caused by inevitable deviation from vertical etching of the sidewall), at these positions the gate

electrode cannot be in direct contact with the 2DEG.

In order to formulate the PF process at the mesa sidewall, the electron emission is in here assumed to take place from a trap state close to the gate metal at the mesa-sidewall into a continuum of states in GaN. It is then through this continuum of states that electrons reach the 2DEG [59], [80]. The damage caused by inductively-coupled plasma etching (ICP), which is used to form the isolation-features, contributes to the formation of the aforementioned traps close to the sidewalls. The PF current density is presented by [13], [80],

$$J_{PF} = C_{PF} E_{sidewall} exp\left(-\frac{q(\phi_t - \sqrt{qE_{sidewall}/\pi\varepsilon_0\varepsilon_s})}{kT}\right) \quad (4.6)$$

in which, in addition to the aforementioned parameters, ε_s is the relative high frequency permittivity of GaN, $q\phi_t$ is the barrier height for electron emission from the trap state, and C_{PF} is a constant.

In (4.6), $E_{sidewall}$ is the electric field defined in terms of the potential difference between gate and the 2DEG. This electric field depends on several parameters including the slope of the sidewall and the strain relaxation at the vicinity of the mesa edge. The maximum $E_{sidewall}$ is defined where the gate metal covering the mesa sidewall and 2DEG are at the minimum distance. Considering the exponential dependence of PF on the electric field, $E_{sidewall}$ is estimated as a one-dimensional electric field defined at the depth of the 2DEG channel. However, when considering the fermi-level pinning at the less than vertically defined sidewalls, assuming the linear definition of this one-dimensional electric field in terms of V_{GS} poses considerable challenge on accurate evaluation of the length of the region across which this bias is applied. In the present study, the proportionality factor used in

defining $E_{sidewall}$ in correlation with V_{GS} (here named m_{PF}) is used as the only fitting parameter.

According to (4.6), in the presence of PF emission, ln(J_{PF}/ $E_{sidewall}$) is a linear function of $\sqrt{E_{sidewall}}$, where the slope and the vertical axis intercept are functions of T, respectively presented as,

$$a(T) = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_s}} \tag{4.7}$$

$$b(T) = -\frac{q\phi_t}{kT} + ln\ C_{PF}. \tag{4.8}$$

When (4.6) is applicable, according to (4.7) the plot of a(T) vs. 1/T should present a straight line with a slope capable of providing the value of ε_s, which is projected to 0 at very high temperatures. In addition, the slope of b(t) vs. 1/T should be capable of forecasting $q\phi_t$. Although several studies have claimed the observation of PF emission in GaN-channel HFETs, only a few of them have presented the temperature dependence of these factors [13], [16].

For the experimental data from the fin-variety of the devices indicated in section 4.2 of L_G=0.5 μm, Fig. 4.7(a) shows the linear dependence of ln(I_G/$E_{sidewall}$) vs. $\sqrt{E_{sidewall}}$, while Figs. 4.7(b) and (c) depict the variation of a(T) and b(T) with temperature. On these graphs, since the leakage area corresponding to the gate-leakage at gate-covered mesa sidewalls cannot be exactly defined, I_G has been studied instead of J_G. This will only affect the proportionality constant C_{PF}. While the data presented in Fig. 4.7 across a wide range of temperature satisfies the aforementioned expectations of when the PF process is dominant, the accordingly projected values of ε_s and $q\phi_t$ are respectively equal to 5.35 and 0.31 eV.

These values are quite acceptable [13]. As mentioned earlier, m_{PF} is the only fitting parameter employed for the superbly matched model presented in Fig. 4.7 in terms of the dash lines. In here, the value for m_{PF} has been taken as $2.44\times10^{6}\ m^{-1}$.

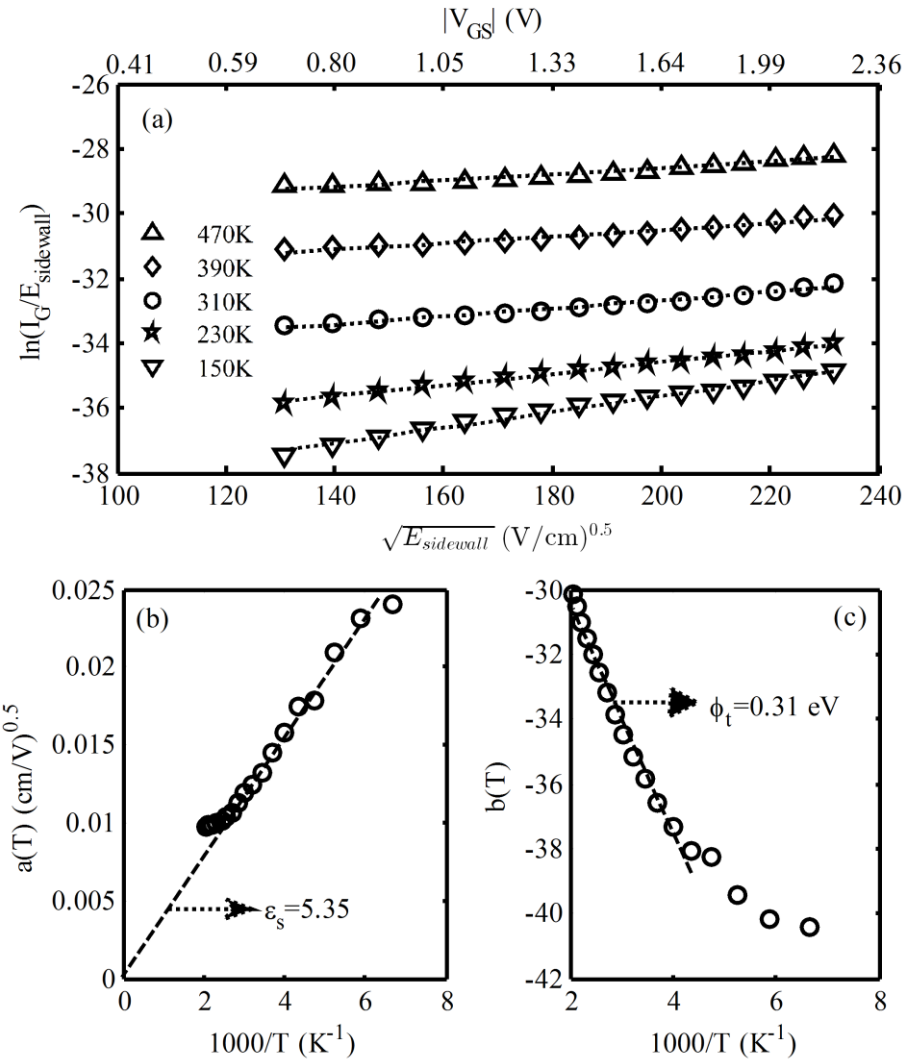


Figure 4.7 (a) $\ln(I_G/E_{sidewall})$ vs. $E_{sidewall}^{0.5}$ over the gate-source regime of bias that the leakage at gate-covered mesa sidewall is dominant. Symbols represent experimental data points. Dash lines are the fitted lines for the presented symbols according to (4.6). (b) and (c) present the slope and y-intercepts of dash lines in (a) vs. 1/T. Only five, out of many temperatures, are presented in (a). V_{DS}=0 V. L_G is 0.5 μm.

Applying the model described in the previous two sections, the calculated I_G over a wide range of values for V_{GS}, for the fin, 7-island, and 14-island variety of AlGaN/GaN HFETs

presented in this chapter, is provided in Fig. 4.8. In this figure, the PF leakage component at the isolation-feature sidewall is calculated for the fin-isolated HFET. The PF component for the 7-island, and 14-island HFETs are considered to be 7 and 14 times larger, respectively. Superb matching between the model and the experimental data (highlighting the turning point between the two dominant processes) suggest the accuracy of the presented model.

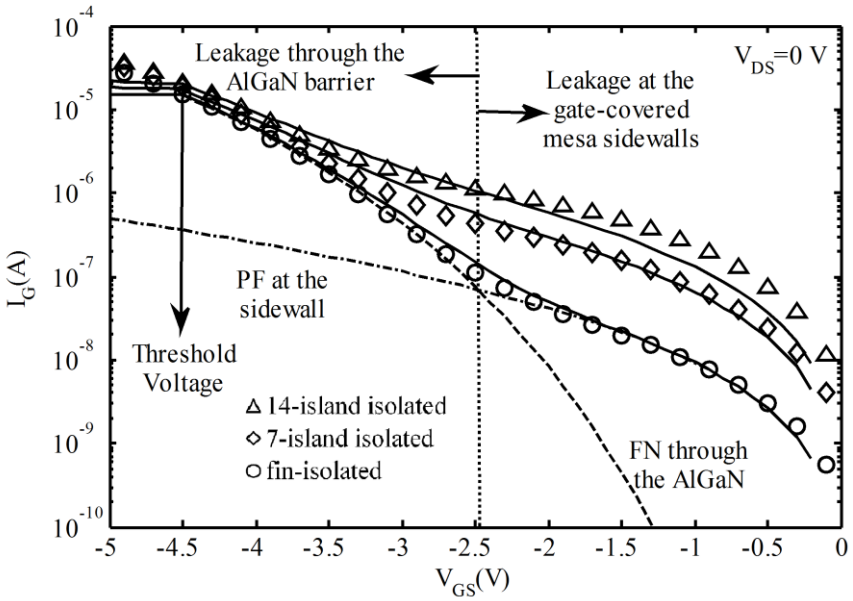


Figure 4.8 I_G vs. V_{GS} over the wide range of V_{GS} for the fin-, 7-island, and 14-island AlGaN/GaN HFET varieties mentioned in section II. Symbols represent experimental data points. Dash line is the calculated FN component through the AlGaN barrier (I_{FN}) discussed in section III. Dash-dot line is the calculated PF at the gate-covered mesa sidewalls (I_{PF}) discussed in section IV for the fin-isolated device. Three solid lines are $I_{FN}+I_{PF}$, $I_{FN}+7\times I_{PF}$, and $I_{FN}+14\times I_{PF}$, which present the total gate leakage calculated for the fin-, 7-island, and 14-island device varieties, respectively. V_{DS} is equal to 0 V and gate-length is 0.5 μm.

4.4 Conclusion

Reverse gate-current of AlGaN/GaN HFET was investigated for a group of devices built on a number of alternative isolation-features of different geometries. Results revealed

evidences on the presence of a leakage path at the sidewalls of the isolation-feature between the gate-metal and the 2DEG.

In an attempt to outline a model with realistic set of assumption for describing the reverse gate-current of GaN-channel HFETs, in addition to the leakage taking place through the III-Nitride barrier, the newly identified path via the mesa sidewalls is considered. According to this model, while for small negative values of V_{GS}, I_G is dominated by PF electron emission taking place between the gate-covered mesa sidewalls and the 2DEG, as the gate-source bias gets more negative FN through the AlGaN barrier becomes dominant. Evidence shows that the FN component occurs only in a small portion of barrier (here referred to as *FN leakage zone*).

Chapter 5

Developing a fabrication process for realization of sub-micron gate AlGaN/GaN and AlInGaN/GaN HFETs

5.1 Introduction

Every microfabrication facility, according to its existing equipment and available chemicals, uses a unique process recipe for microfabrication of III-nitride transistors. The first effort in the area of III-nitride processing at McGill nano-tools micro-fabrication facilities (mnm) was focused on fabrication of optical gate AlGaN/GaN HFETs. In order to realize sub-micron gate III-nitride HFETs at mnm, the mode of lithography process should be naturally changed to electron-beam. According to this change, process recipe and the device layout should be modified in compliance with the mode of lithography. In

this chapter, the process recipe developed for microfabrication of sub-micron gate AlGaN/GaN HFETs (and by extension AlInGaN/GaN HFETs) at mnm is presented.

The following steps are necessary in the modification of the existing optical HFET process to a new process capable of realization of sub-micron gates:

- Designing compatible pattern layout with electron beam lithography (EBL) including appropriate registration marks. Several requirements mostly related to the dimension of patterns should be satisfied in this step based on the specification of the writing machine.
- Choosing the appropriate resist and modifying the resist layer parameters in correlation with the specification of the electron beam (i.e. beam intensity, spot size, accelerating voltage, working distance).
- Revising an applicable registration process among patterns from different steps. This part is the most challenging part of EBL. This is since, the EBL resist is sensitive to viewing with an electron beam. Scanning electron microscope (SEM) mode is often used in EBL systems for the registration.

5.2 Details of the fabrication process for realization of AlGaN/GaN HFET of 0.5 gate length

The process recipe presented in this chapter has been developed for an $Al_{0.25}Ga_{0.75}N$/GaN 25 nm/1675 nm hetero-structure grown on a 4-inch Si-face SiC wafer, purchased from Cree Inc. Prior to the fabrication process the wafers covered with 1.5 μm of MICROPOSIT S1813 photoresist were cut into 2cm×2cm samples using Disco DAD3240 automatic dicing saw.

The fabrication process includes the following major steps: mesa etching, metallization and rapid thermal annealing (RTA) of ohmic contacts (source and drain), deposition of schottky gate, and the contact pad deposition. Among these steps only the gate definition step requires EBL, since it includes submicron features. Depending on the feature size, the other steps can be realized either by photolithography or EBL. While photolithography is faster and less expensive, EBL is easier to modify owing to its mask-less nature. Since this project required several rounds of trial and error prior to arriving at a justified version of the recipe, EBL was chosen for the lithography of mesa and ohmic steps in addition to the gate step. Nevertheless, whereas the dimension of the pads are larger than the maximum dimension of EBL writing field (120 μm×120 μm), photolithography was used for the pad definition. The EBL is performed using a TESCAN MIRA3 SEM equipped with a Nanometer Pattern Generation System (NPGS). MIRA3 is a high performance SEM system which features a high brightness Schottky emitter for achieving high resolution and low-noise imaging. In this system, a high voltage of 20 kV is used for accelerating the electrons. NPGS controls the position of the electron beam of SEM in accordance with a desired writing pattern. This system is used for performing EBL using commercial SEMs in several research fabrication facilities. DesignCAD Express 16 is used for generating the lithography pattern required for EBL.

5.2.1 Pattern design and the registration process

The maximum writing field area of MIRA3 is 120 μm×120 μm, which can be achieved when the magnification of the beam is set to minimum. If a larger area is required for writing a feature, the stage that carries the sample should be moved. The stage position

accuracy after each instant of moving is in the order of 1 μm. However, in the development of the present process recipe for 0.5 μm gate HFETs, 100nm accuracy is desired for the relative position of the gate finger with respect to the drain and source electrodes. Thus, moving the stage after performing the alignment process in each step is not feasible. As a result, the maximum pattern area including the registration marks is limited to the 120 μm×120 μm. Based on the limitation of the area, using a limited number (here two) of registration marks for each succeeding patterning steps is adopted.

The registration procedure is as follows:

- A set of registration marks is printed on the resist-covered sample in the vicinity of the main pattern during the first step of lithography, which is the mesa etching process.
- During each of the next two steps of lithography (i.e. ohmic and gate), one pair of registration marks is monitored using SEM electron beam. The writing pattern will be positioned according to the location of these registration marks, while the stage remains unmoved.
- Considering the limited size of the writing field, if multiple transistors were to be printed on one sample, the registration process should be performed for each individual transistor by moving the stage.

Figure 5.1 presents the designed layout for the fabrication of submicron gate AlGaN/GaN HFETs considering the aforementioned criteria. In this layout, four L-shaped registration marks are placed in the unused portions of the 120 µm×120 µm writing field. As will be explained later, these marks should tentatively maintain a 10 µm distance from the edge of the gate pad and the writing field. The two lower marks in each side of the gate pad are

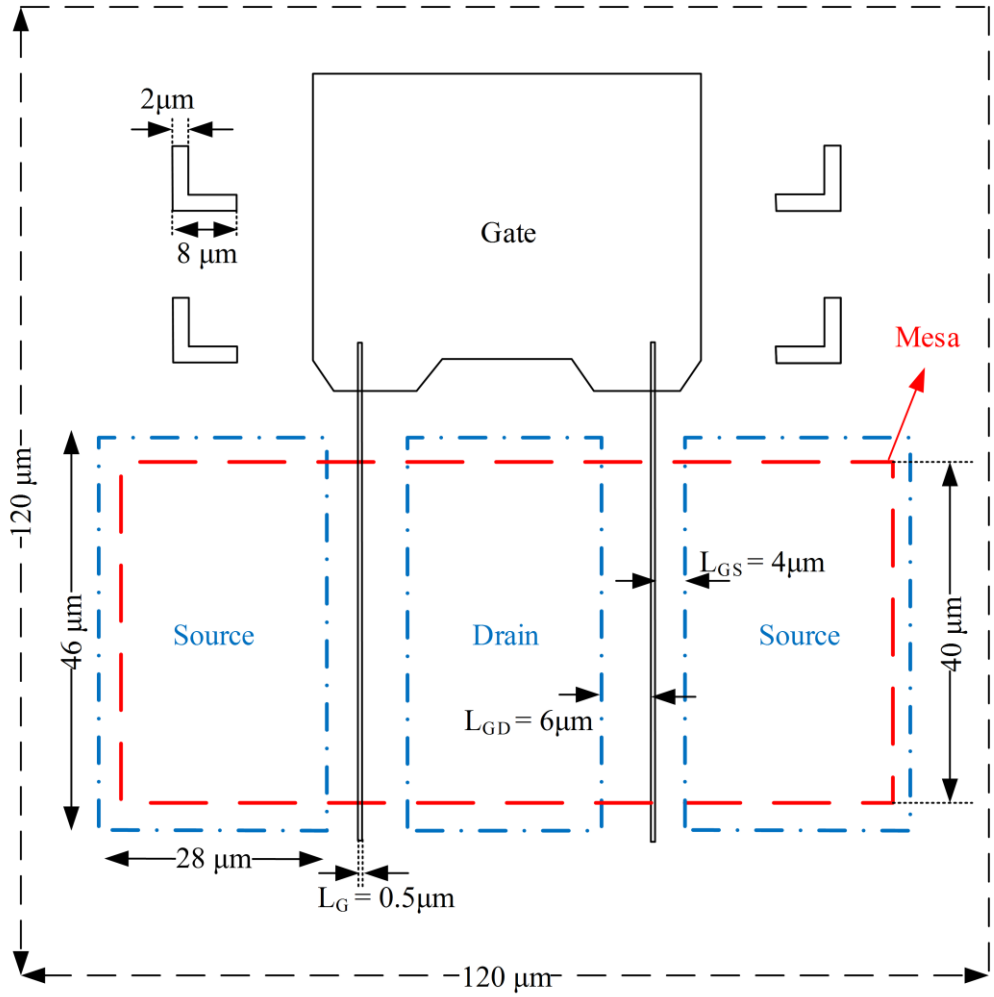


Figure 5.1 The layout designed for the fabrication of a 2-finger submicron gate AlGaN/GaN HFET. The longer dash line indicates the boundary of the Mesa. The dash-dotted lines represent the boundaries of the ohmic contacts. The boundaries of the gate pad and the gate fingers are illustrated by solid lines. The two lower L-shaped registration marks in each side of the gate pad are used for the alignment of the ohmic step, while the two upper marks are dedicated to the alignment of the gate step. Dimensions are indicated on the figures.

used for the alignment of the ohmic step, while the two upper marks are dedicated to the alignment of the gate patterns.

It should be noted that higher accuracy in the registration process can be achieved using larger numbers of registration marks or applying registration marks with smaller dimensions. However, this leads to a longer time for the registration process and an accordingly higher dosage of electron exposure. Since GaN is not a perfect conductive substrate, these electrons can accumulate at the surface of the sample. The accumulated electrons can deviate the electron beam from its designated path. To solve this problem, different remedies are often explored. One such remedy is the deposition of a thin gold layer on the sample prior to the EBL (i. e. electrons evacuation). This solution increases the number of fabrication steps, and also requires a higher voltage for accelerating the electrons. Due to the limitation in the acceleration voltage of MIRA3 SEM, this solution was not explored in this process development. The other solution to decrease the adverse effect of accumulated electrons, is to decrease the timing of the alignment process. This can be done by reducing the SEM resolution during the alignment process. This remedy has been used during the fabrication process presented in this chapter. Furthermore, the distance between the registration marks and the main pattern is designed to be more than 10 μm to minimize the adverse effect of these accumulated electrons on the printing of main pattern.

5.2.2 Writing parameters

After pattern generation using the DesignCAD Express, the patterns are exported to the NPGS to specify the beam maneuver during the EBL process. In this process, in addition

to the pattern layout, a few writing parameters should be defined for the NPGS. These parameters including factors such as exposure area dose, electron beam current, and exposure time, are related through:

$$D = \frac{I_B \times Dwell}{cc \times L_S} \tag{5.1}$$

in which , D is the exposure area dose of the electron beam (C/cm^2), I_B is the electron beam current (A), $Dwell$ is the exposure time for each point being exposed (s), cc is the center-to-center spacing of two adjacent exposure points, and L_S is the line-spacing between the exposure lines. The beam current can be manually adjusted by the SEM control panel. cc, L_S, and D are the input parameters of the writing. These three parameters can be set in an NPGS run file. $Dwell$ is automatically calculated by NPGS through (5.1).

5.3 Process recipe

In the following subsections the major steps of the recipe are presented. A full version of the developed recipe is presented in Appendix I.

5.3.1 Mesa isolation and printing the registration marks

Definition of the active device area, realization of isolation between neighbouring devices, and locating the alignment marks needed for the registration of the upcoming steps can all be performed in one etching step. This step is the first step in microfabrication of AlGaN/GaN HFETs. Since in this step all of the surface area of the sample, except a small portion (i.e. the mesa and registration marks) should be etched, a negative resist is desired for this step.

SU8 is the most common negative photoresist sensitive to UV and electron beam, which is widely used in academic micro-fabrication facilities. The main drawback of SU8 is that, the highly crosslinked epoxy remaining after development of this resist, cannot be easily removed using common solutions such as acetone or MICROPOSIT-Remover 1165 [81]. Moreover, the ashing or dry-etching methods used for the SU8 removal normally burden the surface with residual damage [81], incompatible with this project.

As a result, in place of SU8, ma-N 2400 manufactured by Micro-resist Technology was chosen in this process as the negative resist. ma-N 2400 is a negative tone photoresist series designed for the use in micro- and nanoelectronics. The series is available in a variety of viscosities. The ma-N 2400 is suitable for the residue free removal using acetone or other common removers. In order to make sure that the resist manifests sufficient dry etching resistance, the version with the highest viscosity was selected in this process development. This version which is ma-N 2410 generates a 1 μm thick layer using the normal coating process proposed by the manufacture (which is coating at 3000 rpm for 30 s).

The process flow modified for the application of ma-N2410 in the mesa-etching step of the current fabrication process is presented here:

1. Substrate prepration and coating:
    - Substrate cleaning with acetone, IPA and DI water and drying using Nitrogen gun and hot-plate
    - Spin coating the ma-N 2410 resist with 3000 rpm for 30 s
    - Prebaking at 90°C for 150 s
2. Exposure:
    - Using 20 keV e-beam with the exposure does of 100-200 μC cm^{-2}

3. Developement:
    - Developing in ma-D 525 developer offered by the manufacturer of ma-N2400 for 2-5 mins (ultrasonic bath can be used for smaller feature sizes)
    - Rinsing with DI water and drying
4. Hard bake (optional):
    - If required, the etch resistance and the thermal stability of the resist can be further increased. Hardbaking of the developed resist patterns is suggested on a hot plate at 100 °C for approximately 5-15 min.
5. Resist removal after performing the etching process:
    - Using aceton (ultrasonic bath can be used)

It should be noted that in this process since the large thickness of ma-N resist is comparable to some small feature sizes in the pattern (i. e. according to Fig. 5.1 the 2 μm width of the L-shaped alignment mark), realizing these small features becomes challenging. This is because of the lack of the focus at the resist/sample interface. To solve this issue, the development time was increased up to 3 times the suggested value of the manufacturer, and vibration in an ultrasonic bath was added to the development process. Figure 5.2 for alignment marks and the mesa dimensions of Fig. 5.1, and also a number of smaller size features of different degree of repetition, presents micrographs of the etched patterns. The writing parameters used for the EBL in this step are summarized in Table 5.1. Although Fig. 5.2 demonstrates a successful etching process for the larger dimensions of Fig. 5.1, a relative degradation in the definition of the boundaries is observed when feature sizes get smaller and the distances between them diminish. In correlation to this observation, the

importance of increasing the development time and adding an ultrasonic bath during the

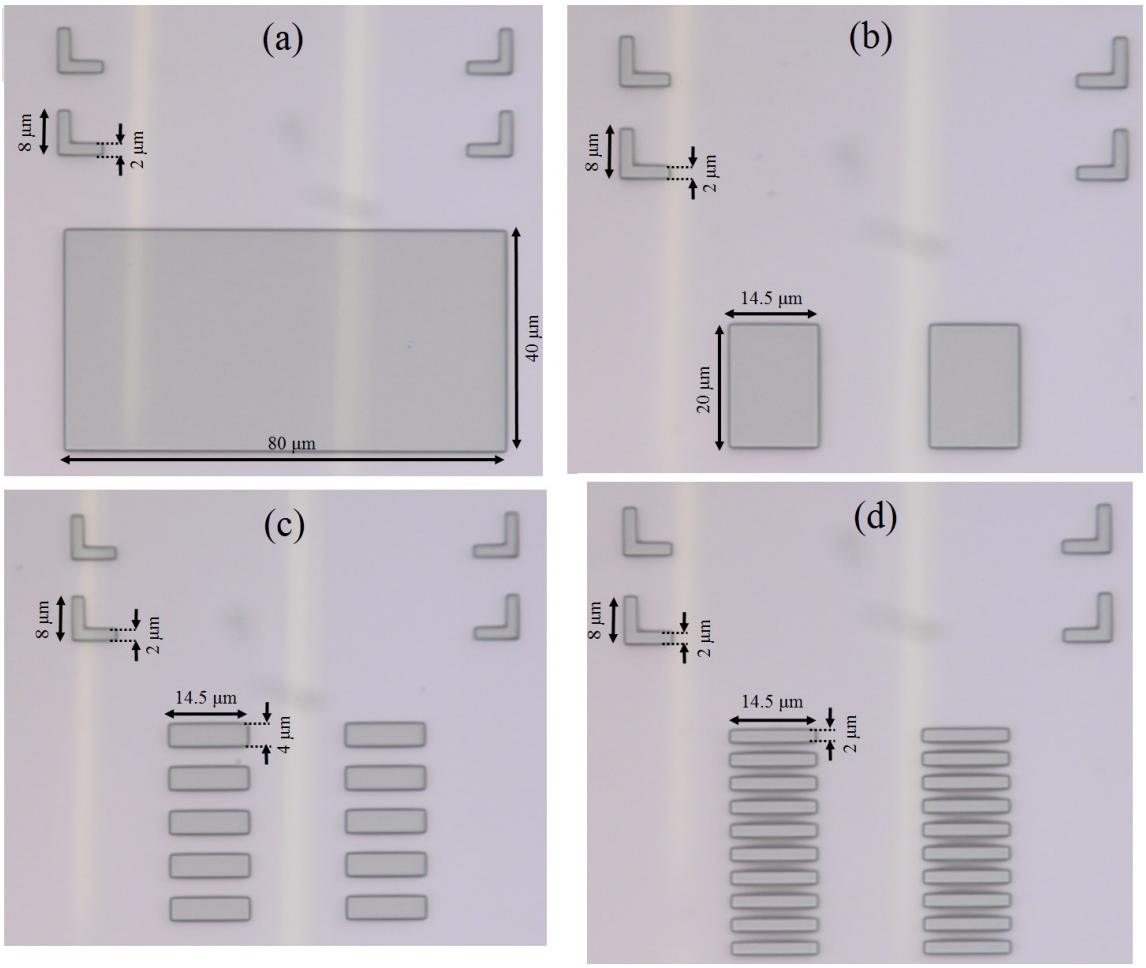


Figure 5.2 Resulting etched patterns of mesa and alignment marks from Fig. 5.1 (a). In (b)-(d) in addition to alignment marks, resulting etched patterns of smaller sizes and with different degree of repetition is presented.

development process can be deduced from Fig. 5.3.

The magnetically-enhanced reactive ion etching (MERIE) by using Cl_2/Ar plasma in an Applied-Materials P5000 MERIE system is used in etching these patterns. Table 5.2 summarizes the adopted parameters in etching based on the prior work in the Reliable Electron Devices group [82], [83].

Table 5.1 Writing parameters used for the EBL of mesa using ma-N2410

Parameter	Value
Exposure area dose	100 μC/cm^2
Beam current	47 pA
Center to center spacing	50 nm
Line spacing	50 nm
SEM working distance	5 mm
Magnification	2000
Absorption current on the sample	39 pA
Spot size	3 nm
High voltage accelerating the electrons	20 kV

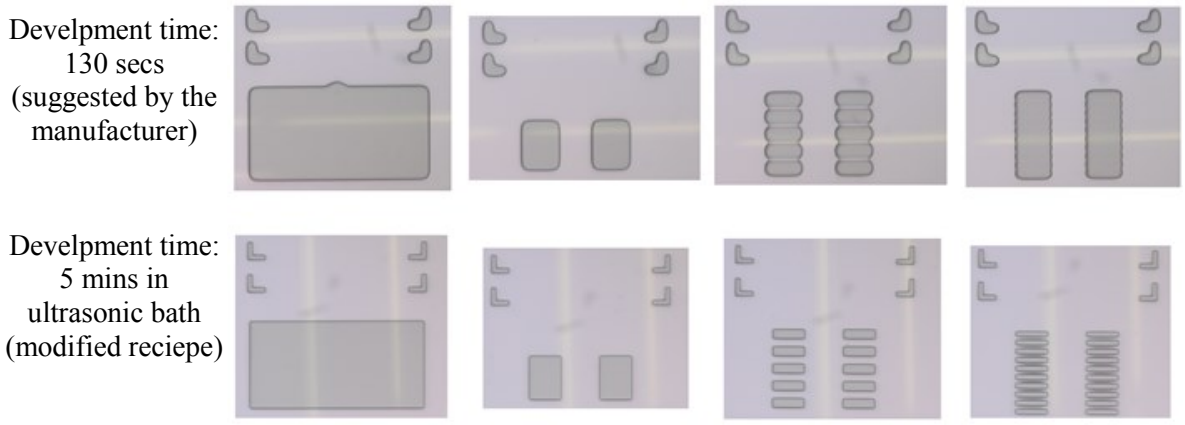


Figure 5.3 The micrograph of etched samples containing features from Fig. 5.2, developed under different conditions. The samples on the top row are developed by the recipe provided by the manufacturer of the ma-N2410. Micrographs shown on the second are developed by the modified recipe explained in section 5.3.1.

Table 5.2 MERIE recipe steps

Step	Cl_2 flow (sccm)	Ar flow (sccm)	Magnetic Field (Gauss)	Power (W)	Pressure (mTorr)	Time (s)
1) Stabilize	20	10	70	0	100	10
2) Etch	20	10	70	170	100	110
3) Ramp down	0	60	0	50	0	10

5.3.2 Ohmic contacts

In order to take full advantage of the properties of AlGaN/GaN hetero-structures, it is essential to realize low resistance source and drain Ohmic contacts to the 2DEG. The process employed for the realization of ohmic contacts in this study includes the following steps:

1. Cleaning with acetone and DI water and dehydration of the sample
2. Coating the sample with MMA(8.5)MAA-EL11 co-polymer/PMMA-A2
3. EBL process
4. Developing the sample in MIBK/IPA 1/3 for 30 s. Stop developing in DI water.
5. Oxide removal at HCl/H_2O 1/4 for 2 mins
6. Metal deposition of Ti/Al/Ti/Au 250Å/1500Å/400Å/250Å
7. Liftoff in acetone using ultrasonic bath
8. Rapid thermal annealing at 850°C for 30 s in N_2 ambient

The bilayer resist scheme of MMA(8.5)MAA-EL11/PMMA-A2 co-polymer/positive resist was used with the goal of easing the lift-off process [84]-[86]. A layer of MMA(8.5)MAA-EL11, which is the lower resolution resist among the two is coated first following by PMMA-A2, a higher resolution layer. In this way, as depicted in Fig 5.4, upon exposure to e-beam the lower resolution of copolymer layer generates an undercut in the pattern. This undercut allows obtaining a good quality lift-off. Using this method, during the lift-off process the solvent (which is acetone in this case) can access all areas of the surface topography and lift-off the resist layers without leaving any residue on the sample. The

thicknesses of the co-polymer/resist layers are identified in Figure 5.4. The coating and baking processes suggested by the manufacture of the PMMA are as follows:

1. Spin coat MMA(8.5)MAA-EL11 resist by:
    - Spread at 500 rpm for 5 s with acceleration of 1305 rpm/s
    - Spin with 4000 rpm for 45 s with acceleration of 1305 rpm/s
    - Deceleration for 5 s
2. Bake sample on hotplate at 150°C for 90s
3. Cool down the sample to near room temprature
4. Spin coat PMMA resist by:
    - Spread at 500 rpm for 5 s with acceleration of 1305 rpm/s
    - Spin with 4000 rpm for 45 s with acceleration of 1305 rpm/s
    - Deceleration for 5 s
5. Bake sample on hotplate at 180°C for 90 s

After coating the bilayer MMA(8.5)MAA-EL11/PMMA-A2 resist, the samples are moved to the MIRA3 chamber for performing the EBL process. The writing parameters used for the EBL are summarized in Table 5.3.

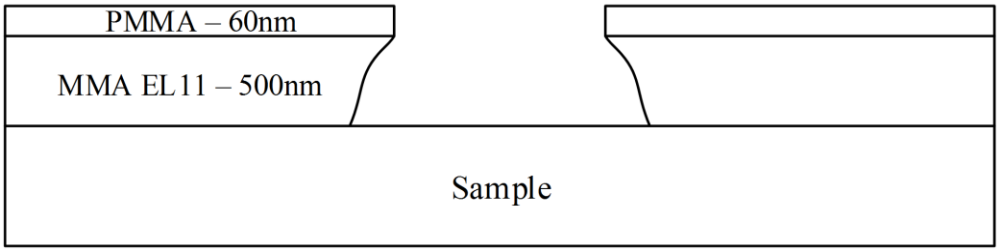


Figure 5.4 The bilayer resist scheme of MMA(8.5)MAA-EL11/PMMA-A2 co-polymer/positive resist used for the EBL of ohmic step. The created undercut applying this bilayer scheme offers good quality lift-off.

Table 5.3 Writing parameters used for the EBL of ohmic contacts using MMA(8.5)MAA-EL11/PMMA-A2

Parameter	Value
Exposure area dose	100 μC/cm^2
Beam current	49 pA
Center to center spacing	50 nm
Line spacing	50 nm
SEM working distance	5 mm
Magnification	2000
Absorption current on the sample	37 pA
Spot size	2.9 nm
High voltage accelerating the electron	20 kV

After EBL, the samples are developed in MIBK/IPA 1/3 for 30 s, immersed in DI water to stop the development process. A post-bake at 100°C for 60 s is applied to remove the residual developer, rinse solvent, and moisture from the resist image.

Prior to the Ohmic contact deposition, the native oxide was removed by dipping the samples in HCl:H_2O (1:4) solution for 2 minutes, then rinsed in DI water and dried with nitrogen gun. This step is performed, since even a thin layer of native oxide can drastically increase the ohmic contacts resistance. The NEXDEP electron-beam evaporator was used for the metal deposition. The metal stack of Ti/Al/Ti/Au 250Å/1500Å/400Å/200Å [87] is deposited under the base pressure of 9×10^{-6} Torr. The metalization process is followed by the liftoff in the aceton using ultrasonic bath.

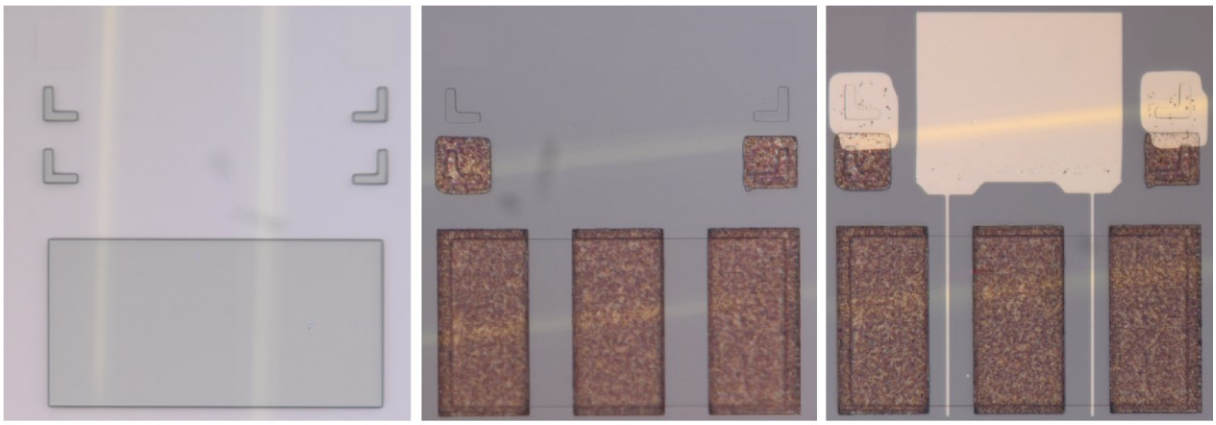
Finally, rapid thermal annealing (RTA) process at 850°C for 30 sec using Qualiflow Therm-JetFirst 200 is used to formed the alloyed ohmic contact to the 2DEG[82], [83].

5.3.2 Gate process

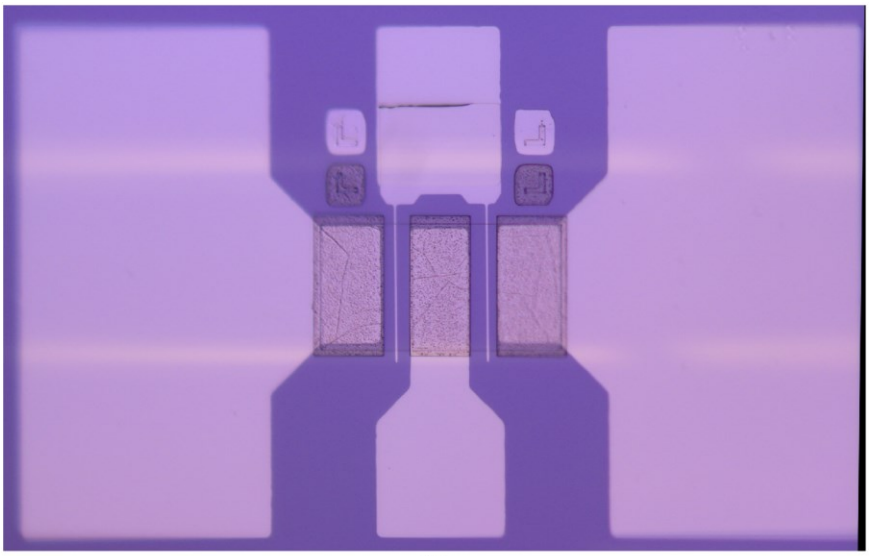
The gate metal is deposited using a similar process to ohmic contact deposition. For the EBL process of the gate, the exposure dose used for the gate pads is 100 $\mu C/cm^2$, however, for the gate fingers the exposure dose of 200 $\mu C/cm^2$ is applied. Other EBL parameters are similar to the ones indicated in Table 5.2. Development in MIBK/IPA 1/3 for 30 sec and a post-back at 100°C for 60 sec are followed by the metallization of Ni/Au 200Å/200Å gate metal stack using the NEXDEP electron-beam evaporator. Then a standard lift-off process in aceton using ultrasonic bath is performed.

5.3.3 Pad deposition

As mentioned earlier in section 5.2, because of the large dimensions of pads optical lithography is used for the definition of this layer. EVG620 mask aligner is used to align the optical mask of the pads with the previously generated patterns. Image reversal lithography using AZ5214 (and developer AZ726) is used in this step. The details of the lithography are similar to the previous process recipe used in the group [82], [83]. The e-beam evaporated metal stack of Ni/Au 200Å/300Å is used for the pads. Figure 5.5 illustrates the micrographs of a fabricated transistor after each major individual fabrication step.



(a) (b) (c)



(d)

Figure 5.5 Micrograph of a fabricated transistor after each of the major fabrication steps (a) Etching of the mesa and two sets of L-shaped registration marks. (b) Deposition of ohmic contacts. The surface morphology of the ohmic contacts becomes rougher after RTA. (c) Deposition of the features at the gate step. (d) Deposition of pads. Parts (a)-(c) are performed using EBL, while (d) is realized using optical lithography. Dimensions are as ones indicated in Fig. 5.1.

5.4 Characterization

In the following subsections the result of DC characterization and DC stress test are presented.

5.4.1 DC characterization

SÜSS MicroTec PM5 probing station and keithley 4200-SCS semiconductor characterization system have been used for on-chip characterization of the fabricated AlGaN/GaN HFETs explained in section 5.3.

Figure 5.6 shows the typical drain and gate current-voltage characteristics of the fabricated transistors. A superb saturation along with the maximum drain current density of 557 mA/mm is observed. The effects of gate-source and gate-drain access region resistances caused by large gate-source and gate-drain spacing (i.e. 4 μm and 6 μm), are among the reasons for lower than expected drain current density observed for this HFET.

According to the transfer characteristics of the HEFT presented in Fig. 5.7, the threshold voltage of the device is measured to be about -3.6 V. This value is in agreement with the theoretical values calculated in chapter 2 of this thesis for the AlGaN/GaN HFETs with the aluminum mole fraction of 0.25. The maximum extrinsic gate transconductance is 140 mS/mm. The very wide pick of transconductance provides a linear gain, when the HFET is used as an amplifier.

Figure 5.8 shows the sub nano-ampere gate current of the fabricated HFETs vs. the gate voltage. According to the discussion presented in Chapter 4, the small observed gate current demonstrates the good quality of the epilayers. Furthermore, the small gate leakage affirms the high quality of MERIE used for the mesa isolation.

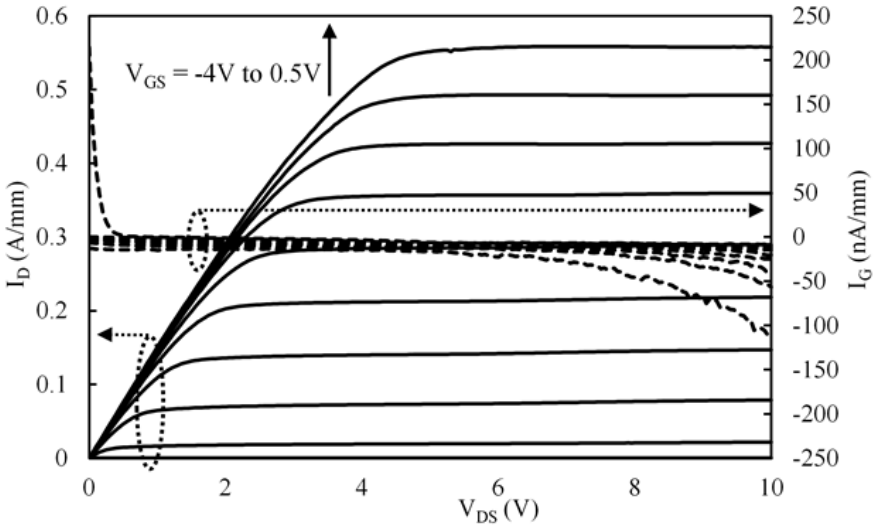


Figure 5.6 Typical drain and gate current density versus drain-source voltage of the fabricated AlGaN/GaN HFEs.

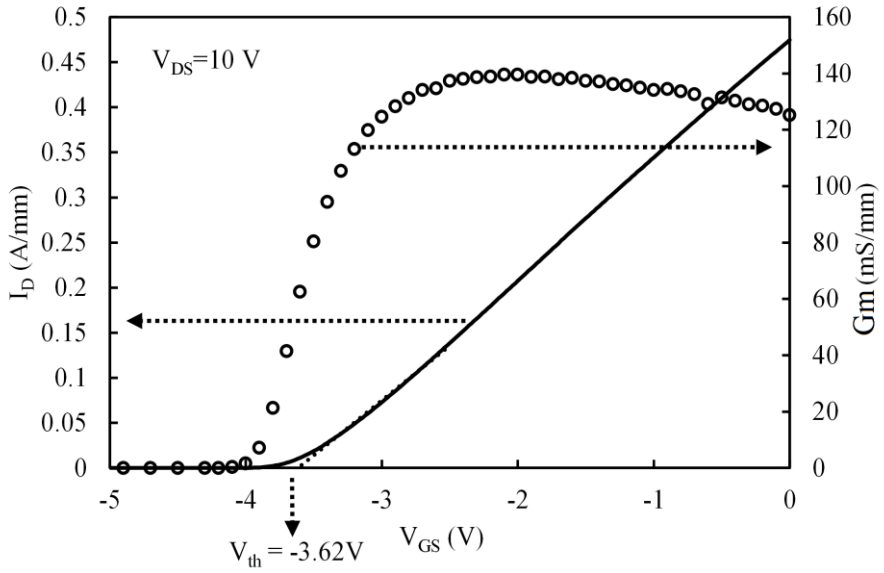


Figure 5.7 The typically observed linear transfer characteristics of the fabricated AlGaN/GaN HFET.

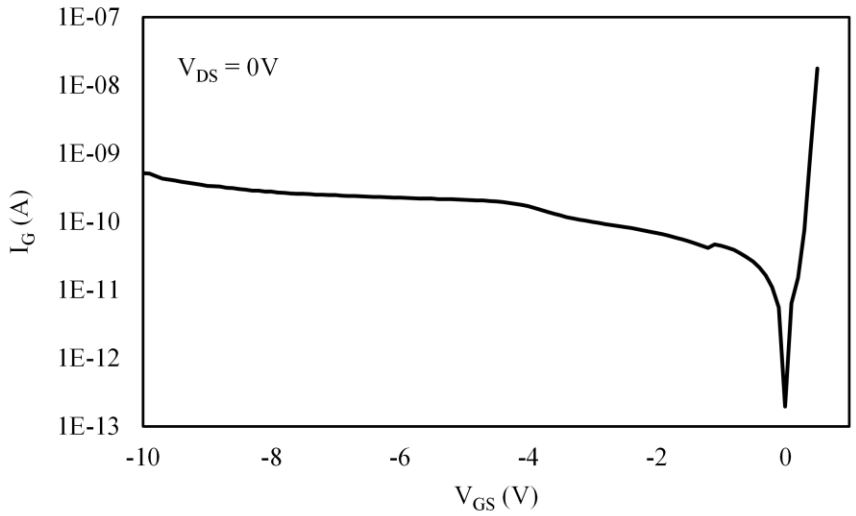


Figure 5.8 Typical gate current vs. gate-source voltage of the fabricated AlGaN/GaN HFET.

The typical observed log-scale transfer characteristic of the fabricated HFET is presented in Fig. 5.9. The subthreshold swing is observed to be as low as 107mV/dec and I_{on}/I_{off} reaches 3.7×10^7. Table 5.3 compares the DC characteristics of the fabricated devices in this chapter, with a similar group of AlGaN/GaN HFETs fabricated by Canadian microelectronics corporation (CMC) microsystems used for the modeling of the gate-leakage presented in chapter 4. Although the barrier specifications (i.e. Al mole fraction and barrier thickness) among these two groups of devices are slightly different, one can still observe through Table 5.1 that the fabrication process developed in this work could meet the quality level of semi-industrial fabrication processes.

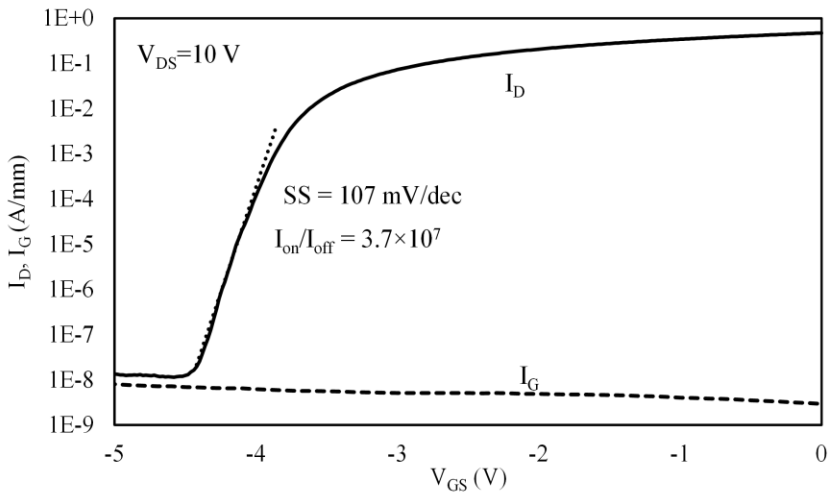


Figure 5.9 Subthreshold characteristics of the fabricated AlGaN/GaN HFET.

Table 5.4 Characterization results summary for the device fabricated in mnm and the ones fabricated by CMC

Parameter	**HFET fabricated in this work**	**HFET fabricated by CMC**
structure	$Al_{0.25}Ga_{0.75}N$/GaN 25nm barrier SiC substrate	$Al_{0.3}Ga_{0.7}N$/AlN/GaN 20+1nm barrier SiC substrate
Gate length	0.5 µm	0.5 µm
V_{th}	-3.64 V	-4.35 V
Drain current density at V_{DS}=10 V	557 mA/mm	700 mA/mm
R_{on} at V_{DS}=10 V	17.95 Ω/mm	14.29 Ω/mm
gm maximum	140 mS/mm	200 mS/mm
I_G at V_{DS}=0 V and V_{GS}=-6 V	0.2 nA	50 µA
SS at V_{DS}=10 V	107 mV/dec	304 mV/dec
I_{off}	15 nA/mm	1.01 mA/mm
I_{on}/I_{off}	3.7×10^7	691

5.4.2 Effect of DC stress

To test the reliability of the fabricated HFETs, a 5hour long DC stress test was applied to the samples. Under the stress condition the transistors were biased at V_{GS}=-2V and V_{DS}=40V. Under this condition the I_D of the fresh device is found to be around 4.5mA. The choice of V_{DS} and V_{GS} are limited due to the voltage and current compliance of keithley 4200-SCS semiconductor characterization system used for the characterization of the devices.

Since the surface of the fabricated devices are not passivated, a relatively rapid degradation occurs under the stress condition. Figure 5.10 compares the I_D-V_{DS} characteristics of the fresh device and the device after 5hr stress. According to this figure, the stressed device shows lower current level in the linear regime and higher knee voltage.

Under the stress condition, electron trapping in the states within the barrier or surface can partially deplete the 2DEG and consequently reduce the channel conductivity of AlGaN/GaN HFETs [88]. In the linear regime of operation, the existence of a region with high resistance in series with the gated channel resistance in the stressed device will cause the current level to reduce and the knee voltage to increase. The fact that the drain current in the stressed device eventually saturated to the same maximum level as the fresh device, although at a much higher drain–source voltage, suggests that the ohmic quality of the drain and source contacts was not degraded by DC stress.

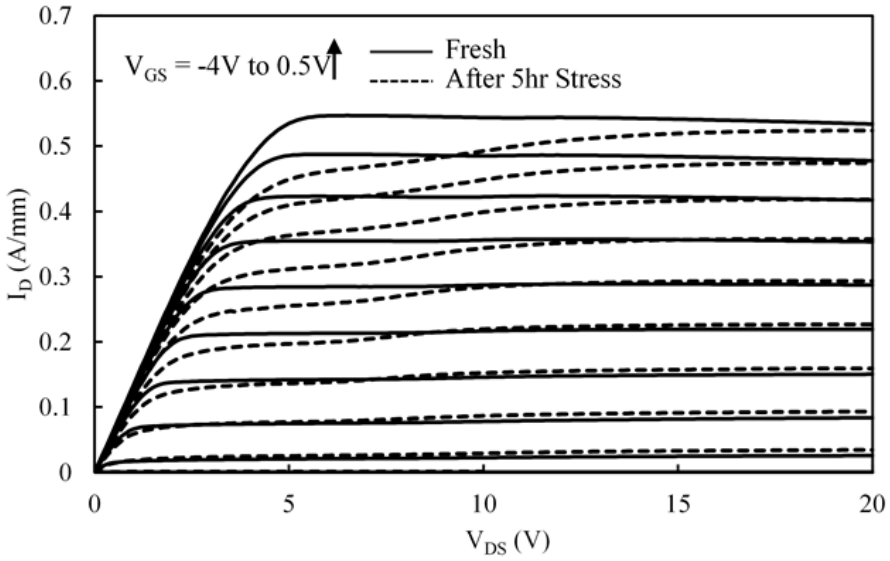


Figure 5.10 Drain I-V characteristics for the fabricated AlGaN/GaN HFETs, before and after DC stress.

Figure 5.11 shows the degradation of the extrinsic gate transconductance of the device by DC stress. The reduction of the Gm at higher values of V_{GS}, when the drain current is higher, is more severe. Figure 5.11 also shows that the DC stress does not shift the threshold voltage, which is in agreement with the results presented in similar studies [88]. Upon application of a series of 5 hour long periods of stress, Fig. 5.12 shows the gradual reduction of the gate transconductance during the stress period. Also on this figure, the gate transconductance after of rest is presented. It should be noted that the gate current and the subthreshold characteristic of the devices did not demonstrate significant change upon stress.

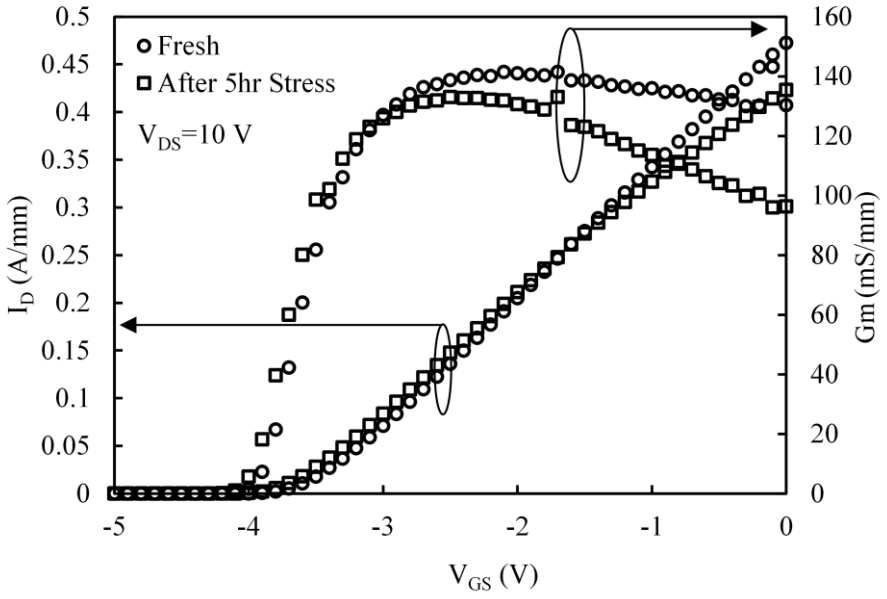


Figure 5.11 Transfer characteristics for the fabricated AlGaN/GaN HFET, before and after DC stress.

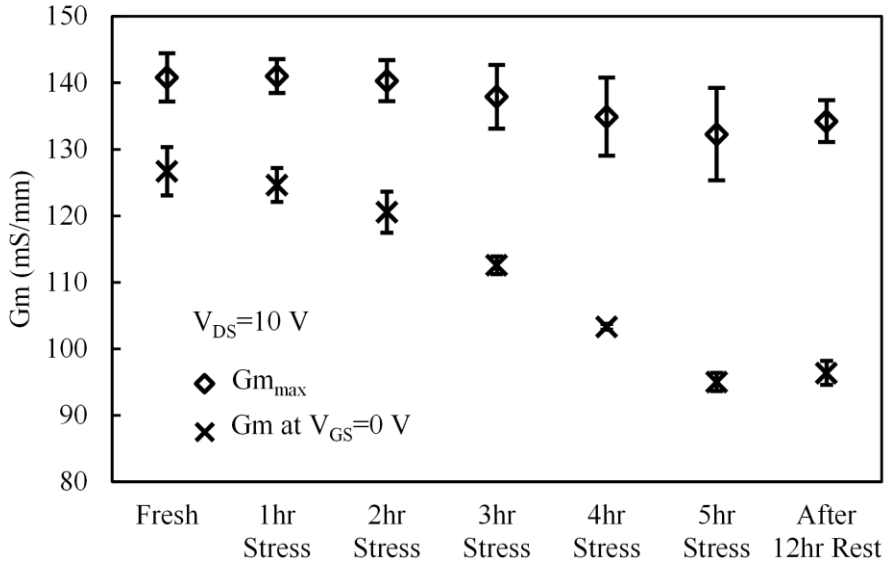


Figure 5.12 Maximum Gm and Gm at V_{GS}=0 V for the fabricated AlGaN/GaN HFETs, before and after DC stress. Symbols represent the average of experimental data points, while the bars provide the range of variation among a number of identical devices.

5.5 Process recipe development for fabrication of AlInGaN/GaN HFETs

The most important modification needed for the process recipe to realize submicron gate III-N HFETs was changing the lithography process from optical to EBL. This modification has been successfully done and has been discussed in this chapter. In this project since we did not have any available AlInGaN/GaN wafers, the fabrication process recipe was performed only for ternary AlGaN/GaN HFETs. A similar process recipe presented in this chapter can be used for the fabrication of quaternary AlInGaN/GaN HFETs with minor modification, especially in terms of RTA process for realization of ohmic contacts. Theoretical studies presented through chapter 2 and 3 can be used to design the layer structure of AlInGaN/GaN HFETs, while the developed process recipe presented in chapter 5 is used for the fabrication process.

5.6 Conclusion

Process recipe using EBL was developed for microfabrication of submicron AlGaN/GaN HFETs at McGill nano-tools micro-fabrication facilities. The fabricated AlGaN/GaN HFET with gate length of 0.5 μm demonstrated maximum drain current density of 557 mA/mm, extrinsic gate transconductance of 140 mS/mm, subthreshold swing of 107 mV/dec and I_{on}/I_{off} ratio of 3.7×10^{7}.

Chapter 6

Concluding remarks, contributions, and future work suggestions

The research direction of this thesis focused on fabrication and physics based modeling of polar AlGaN/GaN and AlInGaN/GaN HFETs. The three objectives of this research thesis were:

- Devising a physics-based model for the gate leakage of AlGaN/GaN HFETs.
- Formulating a theoretical variational model for 2DEG characteristics of AlInGaN/GaN quaternary HFETs.
- Developing the fabrication process for realization of sub-micron gate AlGaN/GaN and AlInGaN/GaN HFETs.

6.1 Concluding remarks

In chapter 2, the 2DEG characteristics of AlInGaN/GaN hetero-junctions were theoretically modeled using the variational method. It was confirmed that the threshold voltage of a

quaternary GaN-based hetero-junction can be increased to values above zero by engineering both the spontaneous and the piezoelectric polarization. Furthermore, this study revealed that in obtaining this end-goal, reducing the polarization through attempting a polarization-matched hetero-structure is not capable of offering the chance of channel formation on the GaN side of the hetero-junction. Hence, a coordinated use of relatively thin barrier (i.e., to enhance Schottky depletion) and strain engineering via incorporation of In in the barrier is needed to warrant a positive threshold voltage. The calculated 2DEG concentrations based on the present theoretical evaluation are in agreement with the experimental values reported in the literature. Results showed that the first and second subbands become closer and the position of fermi level lowers as In mole-fraction increases or Al mole-fraction decreases.

In chapter 3, based on the simulations performed using the commercial Poisson-Schrödinger solver *Nextnano*, a quaternary lattice-match AlInGaN bilayer barrier/spacer design for GaN-channel HFETs was presented. Accordingly, it was shown that this layer structure has the possibility of offering enhancement-mode operation, while allowing good carrier confinement at substantial gate overdrives. Since the proposed barrier/spacer stack is fully lattice-matched to the GaN channel, it also allows for relieving some of the difficulties often attributed to strain relaxation and long term reliability of these polar III-Nitride hetero-structures.

In chapter 4, reverse gate-current of AlGaN/GaN HFET was investigated for a group of devices built on a number of alternative isolation-features of different geometries. Results revealed evidences on the presence of a leakage path at the sidewalls of the isolation-feature between the gate-metal and the 2DEG.

In an attempt to outline a model with realistic set of assumption for describing the reverse gate-current of GaN-channel HFETs, in addition to the leakage taking place through the III-Nitride barrier, the newly identified path via the mesa sidewalls was considered. According to this model, while for small negative values of V_{GS}, I_G is dominated by PF electron emission taking place between the gate-covered mesa sidewalls and the 2DEG, as the gate-source bias gets more negative FN through the AlGaN barrier becomes dominant. Evidence shows that the FN component occurs only in a small portion of barrier (here referred to as *FN leakage zone*).

In chapter 5, process recipe using EBL was developed for microfabrication of submicron AlGaN/GaN HFETs at McGill nano-tools micro-fabrication facilities (mnm). The fabricated AlGaN/GaN HFET with gate length of 0.5 μm demonstrated maximum drain current density of 0.557 mA/mm, extrinsic gate transconductance of 140 mS/mm, Subthreshold Swing of 107 mV/dec and I_{on}/I_{off} ratio of 3.7×10^{7}.

6.2 Contributions

The contributions of this research works are as follows:

Chapter 2:

- Founded on the model presented in chapter 2, this PhD thesis confirmed that the enhancement-mode quaternary AlInGaN/GaN can be realized using polarization engineering of the barrier layer.

- For the first time, this study revealed that in contrary to the previously claimed possibility of offering polarization-matched quaternary hetero-junctions while retaining the large bandgap of the barrier-layer and the resulting proper carrier confinement, this structure is

not capable of implementing this twofold characteristic simultaneously. For a polarization-matched barrier-layer, the buffer/channel layer exhibits a larger bandgap, which rules out the possibility of developing a quantum-well at the hetero-interface. Therefore, no carrier confinement exists in this condition. Although exact matching of polarization is not possible, quaternary barriers can still help design devices with low interface polarization charge.

Chapter 3:

- A quaternary bilayer lattice-match $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N/Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N/GaN$ layer structure were proposed for improving the carrier confinement in the channel of enhancement-mode metal-face c-plane wurtzite AlInGaN/GaN HFETs for the first time.

- Based on the simulations performed using *Nextnano*, while the proposed layer structure substantially improves the carrier confinement in the GaN channel layer, it also upholds the merits of employing a lattice-match barrier towards achieving an enhancement-mode operation.

Chapter 4:

- Evidences on the presence of a leakage path at the sidewalls of the isolation-feature between the gate-metal and the 2DEG have been presented for AlGaN/GaN HFETs.

- A model considering different leakage paths (including the one at the mesa sidewalls) for describing the reverse gate-leakage in polar GaN-channel HFETs was presented for the first time.

- The novel contribution of the model presented in chapter 4 is that it postulates that in absence of absolute uniformity, FN tunneling takes place through only a small portion of

the surface of the barrier, which boasts the highest electric field or the smallest Schottky barrier height. By applying this hypothesis, the origin of the inconsistencies inherent to the previously presented models in selecting the value of the electron effective mass can be explained.

Chapter 5:

Process recipe for microfabrication of submicron gate AlGaN/GaN HFETs using EBL was developed and adjusted at McGill nano-tools micro-fabrication facilities for the first time. The fabricated AlGaN/GaN HFET with gate length of 0.5 μm demonstrated maximum drain current density of 557 mA/mm, extrinsic gate transconductance of 140 mS/mm, subthreshold swing of 107 mV/dec and I_{on}/I_{off} ratio of 3.7×10^{7}.

6.3 Future work suggestions

The following future works are suggested for the continuing study of III-nitride HFETs.

1. Fabrication of bilayer lattice-match $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N/Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$/GaN HFETs

Chapter 3 presented the theoretical discussion on the 2DEG characteristics, with a focus on the carrier confinement and threshold voltage, of bilayer lattice-match $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N/Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$/GaN HFETs. A similar fabrication process presented in the chapter 5 can be applied to the wafers employing this bilayer barrier structure to realize the HFETs capable of offering larger carrier confinement and threshold voltage in the comparison with the conventional quaternary $Al_xIn_yGa_{1-x-y}N$/GaN HFETs.

Characterization of different metal layer schemes for realization of source/drain ohmic contact in $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N/Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N$/GaN HFETs is another contribution to this thesis. Since the bandgap of the $Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N$ part of the barrier is smaller than the one in traditional AlGaN/GaN HFETs, lower temperature of the RTA can be applied in fabrication of these novel transistors.

2. Presenting a more comprehensive model for the sidewall leakage considering the effects of mesa sidewall slope, drain-source voltage, 2DEG electron concentration, and strain relaxation

Chapter 4 focused on the modeling of gate leakage when V_{DS}=0 V, however, the modeling of I_G as a function of V_{GD} has been remained untackled. It is expected that mesa sidewall leakage decreases at higher drain voltage. This is since the 2DEG at the mesa sidewall is depleted easier at higher drain voltage and the distance between the gate and 2DEG on the 2DEG plane expands. At higher values of V_{DS}, the gate leakage is mostly dominated by the vertical leakage component from gate to 2DEG (probably FN), at the drain side of the gate, where due to the positive voltage of 2DEG, the electric field across the AlGaN barrier is maximum. Moreover, the effect of the slope of mesa-sidewall, 2DEG concentration and strain relaxation on the mesa-sidewall leakage can be studied.

3. Suppression of Suppression of gate-leakage in FN leakage zone using modified device structures such as employing the field-plate

As discussed in the chapter 4, FN leakage zone is a portion of barrier which boasts the highest electric field or smallest Schottky barrier height. At large values of V_{DS}, the drain side of the gate would be the main contributor to the FN due to the more positive potential

of 2DEG at this part. Employing modified device structures such as employing gate field-plate can suppress the large component of FN at the drain side of the gate by reducing the vertical electric field across the barrier.

4. Employing the presented in-house fabrication-recipe for realization of devices built on isolation-features with sub-micron feature size

Applying minor modifications in the fabrication recipe presented in chapter 5, this recipe which employs E-beam lithography is capable of realizing the HFETs built on isolation-features with sub-micron feature sizes. These devices can be used for increasing the gate-control effect and applying positive-shift in threshold voltage while they can also reduce the self-heating effects.

5. Study the degradation effects in quaternary HFETs

One major drawback in quaternary HFETs discussed in chapter 2 and 3 of this thesis work can be the long-term reliability of these quaternary HFETs. Although HFETs introduced in chapter 3 take advantage of lattice-match structure, the smaller ΔE_C in these devices in comparison with ternary AlGaN/GaN HFETs may lead to increasing the inverse effect of hot electrons, which in turn reduces the long-term reliability of these devices. Moreover, the reliability of In incorporated thin films at high lattice temperatures which is a likely condition in power device applications can be another reliability issue about quaternary HFETs.

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Appendix I: Process Recipe

Mesa isolation

1. Cleaning
   - Methanol
   - Acetone
   - IPA
   - Deionized (DI) water
   - Nitrogen gun
   - Dehydrate on hotplate at 150 ℃
2. Coat sample with Ma-N 2410 resist
   - Spread 500 rpm 5 s
   - Spin 3000 rpm 30 s
   - Deceleration 0 rpm 5 s
3. Softbake at 90 ℃ for 150 s
4. EBL with exposure dose of D=100 μC/cm^2
5. Develop in ma-D 525 for 3-5 min using ultrasonic bath
6. Stop develop in DI water
7. Hardbake at 100 ℃ for 60 s
8. Etch using MERIE P5000
   - Cl_2: 20 Ar: 10 70 G 0 W 100 mtorr 10 s
   - Cl_2: 20 Ar: 10 70 G 170 W 100 mtorr 110 s
   - Cl_2: 0 Ar: 60 0 G 50 W 0 mtorr 10 s
9. Resist removal with acetone and IPA

Ohmic contacts

10. Sample Cleaning
    - Acetone
    - IPA
    - DI water
    - Nitrogen gun
    - Dehydrate on hotplate 150 ℃ for 2 min
11. Spin coat MMA(8.5)MAA-EL11 resist by:
    - Spread at 500 rpm for 5 s with acceleration of 1305 rpm/s
    - Spin with 4000 rpm for 45 s with acceleration of 1305 rpm/s
    - Deceleration 5 s
12. Bake sample on hotplate at 150°C for 90 s
13. Cool down the sample to room temperature
14. Spin coat PMMA-A2 by:
    - Spread at 500rpm for 5 s with acceleration of 1305 rpm/s
    - Spin with 4000rpm for 45 s with acceleration of 1305 rpm/s
    - Deceleration 5 s
15. Bake sample on hotplate at 180°C for 90 s

16. Expose with 100 μC/cm^2
17. Develop in MIBK/IPA 1/3 for 30 s
18. Stop develop in DI water
19. Post-bake at 100°C for 60 s
20. Oxide removal in HCl:H2O (1:4) solution for 2 minutes,
21. Rinse in DI water
22. Drying with nitrogen gun (Do not use hot plate, otherwise thin oxide maybe grown)
23. Metalization Ti 250 Å / Al 1500 Å / Ti 400 Å/ Au 200 Å
24. Liftoff in acetone and ultrasound bath
25. RTA

Time (s)	Temp (°C)	N_2	Sensor
10		On	TC
150	850	On	TC
30	850	On	TC
100		On	TC

Gate Process

26. Sample Cleaning
    - Acetone
    - IPA
    - DI water
    - Nitrogen gun
    - Dehydrate on hotplate 150 ℃ for 2 min
27. Spin coat MMA(8.5)MAA-EL11 resist by:
    - Spread at 500 rpm for 5 s with acceleration of 1305 rpm/s
    - Spin with 4000 rpm for 45 s with acceleration of 1305 rpm/s
    - Deceleration 5 s
28. Bake sample on hotplate at 150°C for 90 s
29. Cool down the sample to room temperature
30. Spin coat PMMA-A2 by:
    - Spread at 500rpm for 5s with acceleration of 1305 rpm/s
    - Spin with 4000rpm for 45 s with acceleration of 1305 rpm/s
    - Deceleration 5 s
31. Bake sample on hotplate at 180°C for 90 s
32. Expose with 100 μC/cm^2 for gate pads and 200 μC/cm^2 for gate fingers
33. Develop in MIBK/IPA 1/3 for 30 s
34. Stop develop in DI water
35. Post-bake at 100°C for 60 s
36. Metalization Ni 200 Å/ Au 200 Å
37. Liftoff in acetone and ultrasound bath

Pad deposition

38. Spin coat AZ5214 photoresist
    1. Spread 500 rpm 5 s
    2. Spin 3000 rpm 30 s
    3. Deceleration 0 rpm 5 s
39. Softbake at 90 ℃ for 55 sec
40. Exposure with 25 mJ/cm^2
41. Postbake at 105 ℃ for 120 sec
42. Flood Exposure with 250 mJ/cm^2 for 0.6 s
43. Develop at AZ726 developer for 30 s
44. Metalization 200 Å Ni/500 Å Au
45. Liftoff
46. Sample Cleaning with acetone, IPA, and DI water